Analog/Mixed-Signal Circuits, Systems and Devices + TxACE
Research Needs: AMS-CSD + TxACE
June 2016

The Semiconductor Research Corporation (SRC) Global Research Collaboration (GRC) program member companies are pleased to release this document that describes the research needs in the thrust of Analog/Mixed-Signal Circuits, Systems and Devices including that for Texas Analog Center of Excellence (TxACE). Incorporated into this document are the SRC GRC Executive Technical Advisory Board (ETAB) priorities, the Analog/Mixed-Signal Circuits, Systems and Devices TAB (AMS_CSD) strategic planning process, and TxACE joint discussions.

The Analog/Mixed-Signal Circuits, Systems and Devices design research needs of the members are described in six major categories:

- Circuit Power/Energy Management/Optimization
- Robust and Reliable Circuit Design
- High Performance Circuits
- Circuits in Advanced and Emerging Technologies
- Bridging Research Across Disciplines
- Circuit Design for Emerging Applications

Each of these major categories is broken down into several sub-categories which describe the need in more detail. Even so, these are written to be broad in nature so as not to restrict the investigator's approach.

Another classification of research needs is also presented, which highlights the member's areas of interest:

- Power Management
- Mm-Wave
- Energy Harvesting
- AMS Compact Models
- Clocking
- AMS Devices
- I/O
- Data Conversion
- RF Baseband
- Sensors
- High Voltage (e.g. motor drive and LED)

The needs in the AMS-CSD design space cover a broad range of applications, including, but not limited to, high performance processors for data centers, low power processors for mobile computing and communication, healthcare devices, and efficient energy usage and management systems. Investigators are encouraged to link the results of their work with a potential application to help describe the relevance of the proposed work.

This needs document is driving the AMS-CSD solicitation. It is issued to universities worldwide, may be addressed by an individual investigator or a research team. Our selection process is divided into two stages. The interested party is requested to submit a brief 1-page white paper. The white paper should clearly identify what can be done in two years, as well as what additionally could be done if a third year is requested. (Please specify the third-year goals separately.) Two-year-only white papers are also acceptable. A successfully selected white paper will result in an invitation to submit a full proposal, with recommendation that the proposal will be written for 2 years or 3 years. These proposals will be further down-selected for research contracts. The number and size of the contracts awarded will be determined by the amount of available funds, and by the number of high-quality proposals.

Investigators who are funded will be expected to publish at top-tier conferences, including but not limited to ISSCC, VLSI, RFIC, ESSCIRC, ASSCC, BCTM, CSICS and CICC. White Papers for all the categories below will be considered for funding. Note that there is no priority assigned to the order of the major categories or the sub categories. Investigators are limited to participation in two white papers in this AMS-CSD solicitation. Submissions should highlight which needs are addressed, such as "C2.1".

CONTRIBUTORS

ARM	Bal Sandhu
IBM	Tod Dickson
Intel	Arindam Saha, Ram Kumar Krishnamurthy
GLOBALFOUNDRIES	Ali Wehbi
Mentor Graphics	Duaine Pryor
NXP	John Pigott & Doug Garrity
TI	Yanli Fan, Jeff Niles, Yongxi Zhang

Further explanation for C5, Bridging Research Across Disciplines:

A number of key elements required for the continued scaling of analog and mixed signal designs require solutions which include strong elements from multiple subspecialties of physics, manufacturing, and circuit design. This scaling also requires new software tools and makes some previously unsolved analog and mixed signal automation problems more relevant. These also spans the disciplines named above as well as software disciplines.

Device models are a critical interface between the underlying technology and integrated circuit design. Combined with circuit simulation tools, good device models significantly improve design productivity and provide insight into the relationship between design choices and circuit performance. Good device models should scale with latest technology advances, be accurate across a wide range of process/operating conditions, and be efficient. These modeling requirements are challenged by the lengthening list of alternative device materials, structures, and increasing process variations: (1) high-permittivity (high-k) gate dielectric, (2) metal gate electrodes, (3) low-resistance source/drain, (4) strained channel for high mobility and now, (5) non-planar FinFETs and 3D packaging. Process variation usually manifests itself as parameter fluctuations in the transistor performance: typically channel length/delay, threshold voltage, transistor parasitics and I-V characteristics. One builds and characterizes appropriate test structures, accurately extracts, and then embeds these variations into a transistor model file. Only then can the circuit designer perform statistical analysis and optimization to try to mitigate performance variability. Rigorous extraction helps process development shed light on the mechanism of variations. The modeling challenge under variation is to identify systematic variation components, develop predictive models for performance analysis, and incorporate them into design tools.

Manufacturing challenges such as double patterning at the 20nm node and below has significantly increased the complexity of the design rules by a factor 100X stretching to 5000 rules in some cases. For Analog/Mixed-signal circuits, we require more attention to layout such as well proximity, poly spacing, critical line widths and higher sensitivity to device matching. As a result, we desire circuit architectures that are more amenable to overcoming these challenges on advanced process nodes.

Regardless of the technology employed (including EUV), lithography, etch, implant, CMP, OPC, and silicon verification would benefit significantly from extreme regularity. The SRC is already supporting research across thrusts into many aspects of advanced technology: advanced material and process development, CAD and design rules for extreme regularity, 3D devices and packaging, and thermal/power measurement and mitigation to name a few. Integrated cooperation with the circuit design community is sorely needed.

In addition to increasing the complexity of physical verification tools and device models, the increasing difficulty of meeting layout constraints, as described above, means that it is more difficult for a layout engineer to meet these as well as the intended function of the circuit. In this context, variation aware partially or fully automated layout for analog becomes a more interesting research area.

Analog and mixed-signal specific automation needs are also seen to be multidisciplinary, requiring both deep analog and deep software expertise. While there is a small overlap with the CADT group needs, this needs document calls out analog and mixed-signal specific needs for automation.

Advancing analog and mixed-signal design, specification and verification beyond manual entry and brute force ad-hoc SPICE is necessary due to a combination of scaling and integration factors. As more analog circuitry is placed on the SoC die that function needs to be verified in the SoC context to a confidence level commensurate with the digital in order to avoid increasing mask respins. On the scaling front, increasing process variation, increasing complexity of analog-digital interfaces, increased sophistication of power regulation and its interactions with digital power modes are all making analog verification more difficult and making layout closure harder to achieve. Analog has been far more difficult to automate than digital. Natively digital approaches have not translated well. A novel natively analog approach may be necessary.

2016 AMS-CSD Needs Categories

C1   Circuit Power/Energy Management/Optimization

This section describes the needs of the members in the area of circuits and architectures for power, energy management, and efficiency improvements. The interest in circuits spans several orders of magnitude in power and energy. Challenges exist at all levels from data centers, racks, line cards, desktops, laptops, mobile processors all the way down to circuits in embedded microcontrollers consuming micro-Watts of active power with nAmps of leakage. Current novel circuits are desired for deeply scaled CMOS devices to improve the state of the art in both active and static current consumption along with management of thermal limitations. On the other end of the power spectrum in the ultra-low powered battery and ultra capacitor driven or energy harvesting application space, challenges remain in key areas such as power/performance scalable analog (ADC's, DAC's, voltage comparators, etc). An example would be an analog to digital converter capable of variable precision conversion with power scaling with the conversion precision. Crystal oscillators and oscillator interfaces needed for accurate time references consume much of the standby power for ULP devices that must wake up on specific time intervals to communicate with mesh networks or perform specific tasks on a schedule. ULP low ppm drift time or frequency references are needed. Another key ULP need is for CMOS nano power current sensors for coulomb counting. Nano power current sensors would have many uses such as voltage regulator or voltage converter control or to monitor and/or allow control of current consumption.

C1.1	Very energy efficient digital and analog circuits
C1.2	High efficiency integrated (e.g. SoC, SiP, 3D) circuits used for power management, including regulators, DC-DC converters, and new control architectures, such as the examples resonant, or SIMO, etc.
C1.3	Thermal management circuitry including high accuracy compact temperature sensors
C1.4	Control/management of leakage current
C1.5	Ultra-low power frequency or time sources (ppm drift rates suitable for real time clock applications)
C1.6	Nano-power current sensor for digital coulomb counting
C1.7	Power/performance scalable analog circuits
C1.8	Fine-grain power management techniques such as state-retention, rapid on/off, etc.

C2   Robust and Reliable Circuit Design

Robust circuit design means designs that meet requirements are insensitive to undesired process and environmental conditions; have high yields and are thoroughly testable. Reliable designs maintain this performance during the product's lifetime. Across the disciplines of analog, digital, RF and memory circuit design, the most traditional way to build robust circuits has been through overdesign; many designs are constructed to overachieve on the highest priority metrics (often speed) when process and environmental parameters are nominal, so that those metrics still meet the desired specs even when degraded by variation in those parameters. The cost of this overachievement is relaxation of lower priority metrics, usually power. Contrastingly, many commercial requirements are to meet minimum performance criteria over all conditions rather than to optimize performance in a narrower range of conditions.

Historically, steady improvement in the tradeoff between performance, area, and power has, however, slowed, while the desire for progress in function/power is as great as ever. At the same time, as supply voltages have become lower and geometries decrease, worst-case variability of device parameters has become more significant. In recent years, robustness has increasingly been achieved by making circuits tolerant to built-in and environmental effects without costly overachievement at nominal conditions. Continued innovation is needed in the design and architecture of these circuits. Member companies are seeking approaches that are robust under variations in global and local process parameters, device mismatches, hard or soft failure of individual components, and under the impact of environmental conditions such as supply and temperature, as well as noise and ESD. In addition, enhanced testability—analogous to IDDQ and scan testing for logic—is desirable for reliable analog and power circuits.

C2.1	Circuits for increased tolerance and adaptability to manufacturing/process variability including parameters with non-Gaussian distributions, such as those that are many deviations away from the mean (6+ sigma)
C2.2	Increasing reliability by design with unreliable components, soft errors and voltage "overstress"; testability including reliable BIST for analog circuits; long term reliability and odometers
C2.3	Noise tolerant (EMC) and aging tolerant circuits/isolation techniques, robust and low- capacitance ESD

C3	**High Performance Circuits**

In the "High-Performance Circuits" category high speed communications links, adaptive/high performance power efficient circuits, high speed interconnects continue to be important needs for members companies. For high-speed I/O, member companies seek a broad array of proposals aimed at extending line rates beyond 50Gb/s over an electrical or optical medium. Important components include power and area efficient circuits and systems operating at speeds beyond 50Gb/s, including drivers, equalizers, optical interfaces, and supporting clocking circuits. Novel signaling/modulation schemes with improved spectral efficiency as compared to non-return-to-zero (NRZ) are important for medium-to-long reach electrical links (50-100cm), along with practical circuit implementations to support such modulation. Another persistent need is high-density, power efficient (<1pJ/bit) I/O systems aimed at communicating over advanced interconnect materials and 3D stacks. Scalable, area efficient, high-performance analog and RF circuits continue to be important with a need for configurable and modular architectures that enable reuse. Circuits and systems to enable short-distance, high-data rate (20-30Gb/s) wireless communication at distances up to 10m are sought. Another ongoing need is for high ENOB, reconfigurable ADCs to support future communication needs, such as cognitive radio systems with heavy DSP content, or I/Os to support a wide variety of channel impairments. High-performance, low-jitter clocking techniques to enable high-date rate wireline and wireless communication systems continue to be of interest. Power and area-efficient digital techniques to enhance analog and RF circuits in highly-scaled technologies are still required. Where possible, supporting these high performance circuits in highly advanced technology nodes (<= 14nm) is desirable.

C3.1	Circuits and systems for high-speed electrical and optical communications links (>50Gbps)
C3.2	High-speed signaling/modulation schemes with improved spectral efficiency
C3.3	High-speed short-distance wireless circuits at very low power
C3.4	High-dynamic-range and/or high-speed data conversion circuits and techniques for communication
C3.5	I/O support high data rate communication over high-density, advanced interconnects
C3.6	Power and area efficient, low jitter circuits for wireline and wireless communication systems
C3.7	Circuits and systems for high data rate wireless communication at distances up to 10m
C3.8	Digitally enhanced analog/RF circuits, PLLs, I/Os, and radios
C3.9	Scalable resolution ADCs for communication systems
C3.10	Automated synthesis, verification and validation methods for communication links, ADCs, DACs, and PLLs

C4	**Circuits in Advanced and Emerging Technologies**

This category highlights the need for circuit design in advanced and emerging process technologies especially that enable aggressive process scaling into the sub-10nm range, 3D integration, and use of advanced CMOS structures. In the design of analog and RF circuits emphasis should be placed on scalable designs that enable transition down the technology node while ensuring that area scales proportionally. This will likely require the use of digital techniques to enhance the performance of the analog and RF. New volatile or non-volatile memory designs are also required while meeting the requirements of performance, power, reliability, and scalability. Circuit designs that utilize emerging memory technologies are also desired. Finally, circuits that are based on compressed sampling techniques are also an area of need.

C4.1	Area efficient analog/RF/Clocking/IO design in scaled "digital" technologies
C4.2	Emerging memory design (volatile or nonvolatile) – high performance and power tradeoffs with high reliability and/or 3D scalability
C4.3	Variation tolerant and area efficient digital circuits with low Ion/Ioff in low head room CMOS processes (e.g. extreme scaled CMOS or high Vt ultra-low power)
C4.4	Low voltage digital and analog circuit design including moderate inversion and weak inversion regions of operation
C4.5	Circuit design techniques with advanced CMOS device structures (e.g. carbon nanotubes, spin torque devices, etc.)
C4.6	Reconfigurable Analog/RF design in processes with non-volatile memory bits/tunable devices

C4.7	Robust, low power interface circuits for 3D integration
C4.8	Test structures that target characterization of new sources of variability, (e.g. FinFET/FDSOI/Nanowire devices, emerging memory elements, III-V Integration and 3D, etc.)
C4.9	Low power logic and circuit design utilizing emerging nonvolatile RAM memory technology
C4.10	Silicon circuits based on quantum principles
C4.11	Low power scalable circuits using compressed sampling technology for application such as wireless sensors
C4.12	Hybrid analog digital information processing, circuits and techniques

C5	Bridging Research Across Disciplines

Continued device scaling faces many issues: (1) increased susceptibility to soft errors such as energetic particle strikes, signal and power-supply noise coupling, and noisy device behavior, (2) hard errors from phenomena such as electro migration, device wear out, and aging (e.g. oxide breakdown, NBTI), and (3) for analog devices, gain decrease, reduced matching, and thermal sensitivity. In all, susceptibility to small fluctuations in the manufacturing process rises dramatically. From the manufacturing side, what actually appears on the wafer is becoming more of a suggestion of what was designed into the GDS. The days of What You See Is What You Get (WYSIWYG) are gone. Solving these issues requires a cross disciplinary approach involving close cooperation between the design, CAD, test, modeling, and process development communities. Operating as isolated silos of expertise is no longer sufficient to address the complexity and find compromises necessary to advance circuit design and the underlying technologies.

Circuits with power devices have distinct needs – distributed and non-uniform thermal and Safe Operating Area (SoA) effects, electro migration, energy capability, testability. Furthermore, there is interest in the use of novel wide bandgap materials in some applications and research that addresses those needs are also included.

High performance passive components have become pivotal in analog and mixed-signal circuits. Sensors with different functions provide the first-hand information from the real world. Functional integration of passives and/or sensors with silicon components that can boost the end system into the next level of performance with potential of reduced cost and improved reliability is of great interest.

C5.1	Semiconductor materials/processes/device and circuit design interactions/co-development, including novel non-CMOS devices, as well as extreme layout regularity
C5.2	Variation-aware device and interconnect modeling in advanced technologies
C5.3	Package and circuit interactions – high frequency, low noise, EMI management, power delivery, stress management and 3D IC heat & temperature management
C5.4	Improved digital and/or analog circuit design optimization and productivity through novel CAD techniques, including, but not limited to, utilizing data mining of process, test, and circuit analysis databases
C5.5	Widely applicable mixed-signal isolation technologies, structures, design rules, and methodology for SoC, SiP and 3D
C5.6	Variation-aware and scalable analog/RF/memory/mixed-signal BIST/DFT circuits
C5.7	Power device techniques including thermal and energy optimization, protection and diagnostic techniques for both the device and load
C5.8	Power devices based on novel wide bandgap materials such as GaN and SiC suitable for high speed and high power switching applications, its drive, control, reliability and compact modeling
C5.9	Analog CMOS improvement in nodes from 90nm and below: higher voltage, lower noise, higher working junction temperature, lower leakage and better CHC/NBTI/EM/etc. performance
C5.10	High performance SiGe HBT scaling beyond 500GHz (both ft and fmax)
C5.11	High performance capacitors and inductors/magnetics that can be monolithically integrated with a Si process
C5.12	Optical, magnetic, mechanical, and chemical sensors that can be integrated with a Si process

C6	Circuit Design for Emerging Applications

There is a need to focus on circuit design driven by several emerging applications. For example, in mixed-signal VLSI circuits, there is a growing need to operate in the millimeter wave and sub millimeter wave frequency regime as well as very wide bandwidth range where design methodologies are immature, thus radical new ideas are needed to develop design capabilities. There is also a need to looking at novel sampling approaches including sub-Nyquist and compressive sensing techniques. Some of these needs are driven by software defined radios and cognitive radios, multi-band multi-standard infrastructure, cellular, connectivity and sensor networks. Similarly, on the ultra-low power side, there is a need to develop circuit techniques that could efficiently utilize low-bandwidth and low-duty cycle operation of sensors to reduce the power consumption down to bare minimum to be powered by energy harvesting circuits. Some of the applications include wireless health monitors, temperature and other sensors, display and motor control. There is a need to look at low-power circuits for RF synchronization and hand shaking methods including wakeup radios, energy efficient wireless power transceivers including antenna and techniques to manage multiple energy sources that may not be well behaved, such as energy harvesting sources. Finally, an additional emerging application need is the area of security with circuits for anti-counterfeiting, random number generation and secure operation.

C6.1	Low power and scalable non-Nyquist and other novel sampling techniques (e.g. compressive sensing)
C6.2	Wearable health monitors: Power efficient body sensor circuitry and/or dry skin contact sensing
C6.3	Efficient and affordable circuits for emerging lighting and display applications
C6.4	Energy efficient wireless power transmit and receive circuits, including the antenna
C6.5	Low power circuits for timing and control of sleep/wake sequences
C6.6	Circuits for managing multiple energy sources that are not well behaved, such as from energy harvesting
C6.7	Energy Efficient Spectrum Sensing for cognitive radio applications
C6.8	Circuits for multi-band/multi-standard, including front-ends (infrastructure, cellular, connectivity or wireless sensor network)
C6.9	Low-power circuits and techniques for RF synchronization and hand shaking including wakeup radios
C6.10	Signal amplification near and beyond fmax for millimeter wave and sub millimeter wave applications
C6.11	Energy efficient motor control and driver circuits
C6.12	Circuits for millimeter and sub-millimeter applications such as IR imaging, communications, and radar
C6.13	Low power circuits and applications utilizing time-based processing
C6.14	Anti-counterfeiting circuitry based on PUF and/or non-PUF techniques
C6.15	Standard process compatible true random number generation
C6.16	Circuits for side-channel attack detection and/or prevention