System, Logic and Physical Design Tools

CADT Needs

Semiconductor Research Corporation

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The Computer-Aided Design and Test thrust of the Semiconductor Research Corporation is seeking innovative research leading to significant advances in system, logic, physical, and system design tools to benefit its member companies. Fundamental advances in tools, techniques and models that reduce cost and time to market, that lead to productivity improvements, and that enable designs higher in "quality" – better performance, lower power, more reliable, etc. – are welcome. This document summarizes member company needs in this area. These are not in priority order.

SLPD
Tools for Design Robustness
D1) Electrically aware design rules and models, including extraction and modeling of manufacturability requirements specific to design needs, design rules for specific design / performance targets, etc.
D2) Tools and models for addressing quality and reliability issues, including back-end and front-end of line aging effects, etc.
D3) Tools for signal integrity analysis and noise mitigation for multiple sources of interference (inductance and other high frequency effects, skin effect, coupling, etc.)
D4) Design and design closure tools that address manufacturability/variability at all levels, including circuit marginality resulting from scaling and environmental effects and 3D
D5) Yield-aware and yield optimization tools including resolution enhancement techniques
D6) Bounded IR drop and power EM closure including stimulus selection and automated fixing of failures in physical design database
D7) Tools that take OPC and DFM into account earlier in the design flow, in logic and physical design
Analog Tools
A1) Tools for analog DFM that focus on critical devices (matched pairs, current mirrors, etc.) and minimize unaccounted exposure to random and systematic variations (e.g., layout dependent effects).
A2) Adaptive optimization methods determining on-the-fly what optimization methods to use based on the topology and design needs, including "designer-in-the-loop" optimization tools.
A3) Tools for modeling and automation of design of multiple passives (MEMS, inductors, capacitors)
A4) Advanced simulation tools for analog design
A5) Analog synthesis (integrated with verification) and optimization, taking into account designer intent
A6) Tools addressing noise in mixed-signal designs
A7) Tools for the evaluation and design of multi-chip SoCs containing AMS and digital

System Tools
S1) Tools for system-level tradeoff analysis and design, incorporating power, yield, thermal, timing, performance, etc., including software, real-time and embedded systems, heterogeneous SoC, SiP, 3D, and silicon-package co-design
S2) Tools, methodologies and models that address concerns at all levels, including power, leakage, thermal, manufacturability, voltage/frequency domains, reliability, safety, efficient monitoring circuits, etc.
S3) Planning, exploration, and design tools for homogeneous/heterogeneous multi-core systems, including innovative and efficient communication fabrics, clock distribution, etc.
S4) Advanced logic/physical/high-level synthesis and cross-boundary optimization
S5) Fundamental/significant place/route improvements, including how to scale the methods for multi-core designs and reliability-aware place and route
S6) Clock distribution design, clock domain crossing, power reduction techniques

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