Research Challenges in CAD and Test
Semiconductor Research Corporation
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The Computer-Aided Design and Test thrust at the Semiconductor Research Corporation is soliciting university proposals in system, logic, and physical design tools; test and testability; and verification to address the challenges below. These challenges have been developed by experts in SRC member companies and have been organized to direct interested parties to appropriate topics. Researchers are encouraged to utilize industry standard tools as a basis or reference point, and to specify clearly not only how their research goes beyond the industry state of the art, but also how they would put their results into practice in an industrial setting alongside existing methodologies and tools.

SRC seeks university research which is pre-competitive, and promotes interaction between faculty and industry to address challenges that members see in future systems and technologies. Unfortunately, only a very small number of proposals will be selected for funding.

Be sure to follow the instructions in the Request for Research when responding.

System, Logic, and Physical Design Tools

S1 Tools for Design Robustness

S1.1 Electrically aware design rules and models, including extraction and modeling of manufacturability requirements specific to design needs, design rules for specific design / performance targets, etc.

S1.2 Tools and models for addressing quality and reliability issues, including back-end and front-end of line aging effects, etc.

S1.3 Yield-aware and yield optimization tools including resolution enhancement techniques

S1.4 Bounded IR drop and power EM closure including stimulus selection and automated fixing of failures in physical design database

S1.5 Tools that take OPC and DFM into account earlier in the design flow, in logic and physical design

S2 Analog Tools

S2.1 Tools for analog DFM that focus on critical devices (matched pairs, current mirrors, etc.) and minimize unaccounted exposure to random and systematic variations (e.g., layout dependent effects).

S2.2 Tools for modeling and automation of design of multiple passives (MEMS, inductors, capacitors)

S2.3 Advanced simulation tools for analog design

S2.4 Analog synthesis (integrated with verification) and optimization, taking into account designer intent

S2.5 Tools for the evaluation and design of multi-chip SoCs containing AMS and digital

S3 System Tools

S3.1 Tools for system-level tradeoff analysis and design, incorporating power, yield, thermal, timing, performance, etc., including software, real-time and embedded systems, heterogeneous SoC, SiP, 3D, and silicon-package co-design

S3.2 Tools, methodologies and models that address concerns at all levels, including power, leakage, thermal, manufacturability, voltage/frequency domains, reliability, safety, efficient monitoring circuits, marginality, robustness, environmental effects, etc.

S3.3 Planning, exploration, and design tools for homogeneous/heterogeneous multi-core systems, including innovative and efficient communication fabrics, clock distribution, etc.

S3.4 Advanced logic/physical/high-level synthesis and cross-boundary optimization

S3.5 Fundamental/significant place/route improvements, including how to scale the methods for multi-core designs and reliability-aware place and route

S3.6 Clock distribution design, clock domain crossing, power reduction techniques

Test

T1 Test Cost and Quality Improvement
T1.1 Test cost reduction
T1.2 Adaptive test
T1.3 Known Good Die and reliability
T1.4 Methods to improve test quality by effective test pattern selection across fault models
T1.5 Burn-in elimination / accelerated stress testing
T2 Yield Learning and Improvement
T2.1 Diagnosis methods to isolate defects and marginalities in digital and mixed-signal systems
T2.2 Methods and metrics to expose subtle, systematic defects and marginalities
T2.3 Statistical techniques to aid volume diagnosis
T2.4 Novel design-for-defect-tolerance (DFDT) methods
T3 Analog, Mixed-Signal, and RF/High Speed Test
T3.1 Methods, including BIST with coverage and test metrics to detect defects/marginalities in analog, high speed, IO, sensors and RF
T3.2 Fast tuning calibration and repair
T3.3 Analog device reliability under stress
T3.4 DfT, BIST, and BIT techniques for analog/mixed signal and Sensors
T4 High-Level Test, Diagnosis and Repair
T4.1 System-level test and in-system debug
T4.2 In-system test techniques for critical applications
T5 Post-Silicon Validation
T5.1 Efficient system-level functional debug
T5.2 Bridging pre-silicon to post-silicon verification; post-silicon validation planning, verification, and debug
T5.3 Silicon validation of mixed-signal systems
T6 Test and Power
T6.1 Test and power management, including low power devices and low power modes
T6.2 Test methods to validate and test for power delivery effects and power modes and /improvement of power integrity during test
T7 Test for New Applications and New Technologies
T7.1 Testing of resilient features and of aggressive/adaptive designs
T7.2 Testing and DFT for 3D
T7.3 Fault models / algorithms / testability requirements for finFETs and finFET-based memories

Verification

V1 Verification Core Technologies

V1.1 Advances in the scalability of automated model checking and sequential equivalence checking techniques for bit-level and bit-vector models

V1.2 Advances in techniques: general-purpose SAT solvers; constraint solving techniques; SAT solvers tuned for specific applications; automatic abstraction and abstraction-refinement; satisfiability modulo theories (SMT)

V1.3 Novel and improved algorithms for optimizing design and specification logic.

V1.4 Effective mechanisms for definition of assertions and coverage from an executable specification language. Coverage visualization methodologies and applications to verification (both digital and AMS) and emulation

V2 System-Level Verification including SoC

V2.1 Verification of communication fabrics, with focus on liveness and non-functional properties such as quality-of-service

V2.2 Validation of SoC system integration, including validation of interface functionality; specification, detection, and validation of constraints arising from HW/FW/SW integration; specification and analysis of system-level flow compliance.

V2.3 Resilience techniques to assess and verify system functionality in the presence of soft or hard errors

V2.4 Co-verification of systems containing hardware and software/firmware components

V3 Analog/Mixed Signal Verification

V3.1 Realistic analog / mixed signal specification, formal verification, equivalence checking, and coverage analysis

V3.2 Methods to help designers create models at various levels of abstraction, and to demonstrate the equivalence or correlation between models at various levels of abstraction. Attention should be paid to readability, maintainability, and particularly debugability of any automatically generated models.

V3.3 Machine learning and data mining applications on AMS circuit behavior and verification

V4 Security and Emerging Applications of Formal Methods

V4.1 Methods and models for hardware security, including the hardware/software interface.

V4.2 Efficient verification of SoC, platform, and system level non-functional properties, especially power, performance, error injection, and safety.

V4.3 Machine learning / data mining / big data analytic techniques for verification, validation, emulation, and diagnosis for functional and non-functional properties