Test Needs to Augment SRC Test and Testability Portfolio

The SRC member companies have identified research needs in test and testability not now adequately addressed in the SRC portfolio. The needs outlined in this document are not a comprehensive list, and do not replace previous needs documents in this area.

Mixed Signal/Analog Test and Testability

Test of mixed-signal and analog circuits is a challenging task and will remain so for the foreseeable future. SRC funded research is seriously needed in this area.

- Fault models, defect models, and measurement methods to discriminate good vs. bad circuits for analog and mixed-signal circuits
- Test metrics (fault/defect coverage and measurement precision) required to provide the quantification needed to define relative quality evaluation for mixed-signal test
- Technical and economic trade-offs between additional analog/mixed-signal tester instrumentation vs built-in circuit testing methods
- Test methods for analog and mixed signal circuit families which utilize the logic testers employed for most SOC chip testing today
- Automatic determination of the boundary between the analog and digital circuits and inserting appropriate test observe and control points for both portions
- Built-in self-test and design-for-test techniques for analog/mixed signal.

These are some of the areas which require research in order to make mixed-signal SOC testing truly viable.

At Speed/AC Testing

The success of scan-based test methods in managing the complexity of testing large chips, along with the increasing difficulty of creating broadside tests for application by expensive high speed testers, requires that on-chip test hardware (e.g. scan or BIST) will be used for an increasing portion of at-speed testing. The nature of high speed circuit design techniques, along with the extra detail required by more complex fault models, presents several new problems to traditional DFT and ATPG approaches that must be solved.

The objective of At-Speed/AC testing methodology is to cost-effectively weed out ICs carrying such defects during manufacturing test screen and provide enough information such that any systemic defects can be quickly diagnosed and the cause of defect be removed. Topics of interest include methodologies and tools for defect and fault modeling, test pattern development, design for test techniques, test equipment and testing interface, development of related design and test automation tools, development of solutions to the currently understood problems and the development of solutions that inherently scale with advancing IC fabrication technologies. Some specific topics of interest are:

- Understanding and characterization of DSM physical defects that may warrant at-speed/AC testing
- Development of surrogate fault models that facilitate easy automatic test development for large ICs without sacrificing the coverage of the underlying defects
- Test development and coverage measurement techniques for cross-talk induced noise and delay
- Practical scan based delay fault test development and test deployment techniques for large ICs
- Techniques for power and noise management during at-speed testing, including limiting power dissipation and managing noise during scan testing or BIST
- Test development methodologies and tools for large ICs with non-homogeneous design and testability characteristic (for example, SoCs)

- Development of "Speed Predictor" circuits and speed co-relation techniques for speed binning of ICs early in manufacturing
- Development of practical surrogate testing methods that provide coverage of defects covered by at-speed testing and AC parametric testing without actually testing at full speed
- Development of suitable DFT and testing methods that reduce or eliminate the dependence on high performance, highly accurate testers, including designing appropriate on-chip testability hardware (e.g., scan or BIST)
- Re-architecting of the test resources on chip, test fixtures and testers that provide at-speed and AC parametric coverage with lower overall cost for several generations of DSM (Test resources partitioning)
- Modeling of high performance circuit types, e.g. dynamic, self-timed, and asynchronous circuits
- Designing appropriate on-chip testability hardware (e.g. Scan or BIST)
- Incorporating accurate timing into test generation models
- Testing across multiple clock domains
- Diagnosis/debug techniques to address AC scan test static and dynamic failures.

Signal Integrity Test

With digital ASIC clock frequencies already in excess of 1GHz, testing for defects that affect signal integrity is becoming critical. To achieve increased circuit density, metal interconnect dimensions are scaled in tandem with device feature sizes. To minimize the circuit performance impact of scaling, interconnect lines are scaled proportionately in lateral dimensions but not in the vertical dimensions, resulting in an increase in ratio of sidewall capacitance to overall capacitance. The increased sidewall capacitance between signal lines (also called cross-capacitance) results in electrical interference between transitioning signals, impacting their waveforms and delays. Depending on the details of the "victim" circuit, noise induced by such phenomena may permanently change circuit state (by disturbing the state of latches or memory elements), introduce delays and eventually result in a fault.

In a typical design environment today, it may not be possible to analyze and fix all such problems with signal analysis tools. In order to insure design fidelity, potentially larger numbers of such problems are handled through very conservative design practices, without explicit verification. For sub-100nm designs, testing techniques will be needed to confirm the design practices. The concerns during testing are accurate speed characterization, establishing frequency shmoo holes (a circuit containing races often works on some frequency bands and not necessarily at all frequencies at or below maximum), and ensuring logical correctness in the established frequency bands.

This is a cross-disciplinary field, ripe for integration of ideas from layout extraction, model order reduction, circuit simulation and testing. The challenges include maintaining consistent data models across layout, transistor, gate and RTL representations, while intelligently trading off accuracy for the ability to handle larger designs across multiple stages of analysis. Testing for cross talk in a hierarchical design environment with embedded cores stands needs to be mentioned separately since it involves the interaction of interconnects within the blocks and the global interconnects. It is quite possible that the analysis tools may not be able to catch this interaction. This also holds true for the embedded memories. Signal integrity issues also arise from inductive effects and the testing should cover these faults also. Similarly, combination of ground bounce and cross talk can potentially create faults which are not realized with only one component present. These faults should also be investigated by testing