SRC Research Needs in Logic and Physical Design and Analysis

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I. Prologue

The research needs document for physical design was first created in draft copy in 1997. This was in response to requests by researchers to identify those areas in physical design of highest concern to industry. A list of the top ten problems as identified by an SRC physical design task force soon followed. This list was then presented to academia and industry at ISPD in April 1999, and at DAC in June 1999 to gather feedback from this list. At ICCAD in November of 1999, EDA was asked to provide their top ten list of problems. Finally in April 2000, we invited EDA, Academia, and Industry to provide their bottom ten list of problems.

In general, this needs document serves the purpose sensitizing the research community to critical needs within physical design. This document has also become very helpful in guiding new researchers to relevant problems. Past documents have also been identified by international researchers as a guide for them as well.

II. Introduction

Research needs in physical design CAD are driven by both constant and changing factors in the design and development of integrated circuits (ICs). The factors that are constant are driven by the industry's desire to continually improve costs while creating more valuable end-user products based on innovative ICs. These factors can be grouped as follows:

- Manufacturing Cost - Minimizing cost through the smaller possible die area, highest possible yield, and reduced test cost.
- Integration - Integrating more transistors and diverse logic types on a single chip, to increase system capability and drive total system cost down.
- Performance - Attaining the best chip and system performance, in particular computing speed.
- Power Dissipation - Minimizing both static and dynamic power.
- Quality - Improving system quality and reliability.
- Design Cycle-time and effort - Reducing the time-to-market and total design cost for new IC designs and incremental redesigns.

Physical design CAD is applied in order to help IC designers meet design feature targets, while minimizing the time-to-market and design effort. As lithography improves along Moore's law path, opportunities for higher performance, greater integration, lower cost, etc. are weighed against design and manufacturing challenges at these new densities. These new opportunities and leverage points for improved IC design create changing sets of possible techniques and technologies for design, influencing CAD research needs. Change factors influencing current physical design CAD research include (but are not limited to):

- Cost - Subwavelength lithography (OPC/PSM)
- Integration - embedded DRAM, mixed-signal, system-on-chip (SoC) design
- Performance - Interconnect dominating global DSM delays, SOI, advanced clocking techniques
- Power - Multi-threshold (Vt) processes, dynamic chip power management
- Quality - Changing testing vs. wafer cost ratio, process variations
- Design cycle-time/cost - Tighter integration of physical design and synthesis

Development of breakthrough physical design CAD techniques would enable more efficient designs for reduced effort and cycle-time. Design flows that require many iterations of physical design improvement, or utilize low-accuracy estimation and analysis, are insufficient for today's designs. Higher accuracy

estimation and analysis techniques that help improve the convergence and reduce iterations should be considered. Higher efficiency of each iteration will speed the overall process.

However, beyond improving the analysis and synthesis in current flows, there is an opportunity to revisit the physical optimization flow itself. Old flow paradigms that separated timing and synthesis from layout have broken down at technology levels where interconnect dominates timing and power. What is needed are new flows that address the new design realities required in current technology without requiring excessive designer effort. This may take the form of algorithms with multi-objective functions which allow of out-of-sequence optimization of the design at any point in the flow. It may include further techniques for integration of layout and synthesis (synthesis-driven layout or layout-driven synthesis). Another approach may be to utilize correct-by-construction methods where layout restrictions and design targets (performance/power) are driven from the synthesis level or even higher levels. The use of design templates where layout flexibility is sacrificed for predictability could also aid in design convergence.

The top research needs list is not meant as an exhaustive list, as all novel techniques that increase designer productivity and improve design results in synthesis, physical design and timing arena are of great interest.

III. SRC Top Needs in Post-RTL CAD Research (Synthesis, PD, and Timing Analysis and Verification)

An original top ten list was presented by Naveed Sherwani at the 1997 International Symposium of Physical Design. While this list was put together by a consortium of professors and industry leaders, a follow on list was created purely from an industry perspective. This top ten list's purpose was to ensure that researchers were sensitized to what the industry rates as important problems rather than what is doable or exciting from a research perspective. The task force that created the list surveyed the research literature, SRC projects, and R&D projects and put forth those problems where current efforts were far behind industry requirements.

This new list extends beyond the traditional lines of digital design. We see SOC chips becoming more prominent as high integration demands stemming from cost and performance demands move the industry in this direction. Hence, the research areas described below include many references to mixed signal and analog designs. These were not broken out into separate design drivers to reinforce the importance of research that comprehends both the high performance digital demands along with the unique demands of analog and mixed signal. The areas listed also define what the "final product" characteristics would be of a tool or group of tools to meet the demands of the design community.

A. Placement and Routing

Summary: A placement and routing solution that considers different circuit families, i.e., digital, analog, etc. as well as their requirements such as performance, signal integrity, reliability, etc.

Description:

For the combined logic and physical synthesis flow to be effective, incremental logic changes must be absorbed seamlessly into the placement and routing domain (see section B for more on this). Algorithmic innovations are needed for placement of thousands of large blocks and millions of small block in a reasonable time. As feature size get aggressively miniaturized, lithography techniques such as OPC and PSM impose additional constraints on the layout and must be considered in P&R. These restrictions bubble up to the routing and even placement domain and present new challenges to physical design. With decreasing feature size comes potential for larger power densities. Placement algorithms which comprehend DFT logic and other low AF modules are needed to disperse these circuits within regions of high power density to create a more even thermal profile. In order to converge to a design solution while meeting performance demands, timing, reliability, signal integrity, and power as well as the clock tree design must be comprehended by the placement and route engine.

Future designs will demand greater integration of digital, analog, and RF. Placement, therefore, must account for timing and noise characteristics of analog blocks in a mixed-signal IP block as

well as contamination of sensitive analog signals from digital signals due to cross talk and substrate noise. If true placement of analog and mixed signal blocks is to be accomplished below the IP block level, then P&R solutions must comprehend symmetry requirements and other analog layout techniques as well as corresponding signal integrity and reliability constraints including IR drop and electro-migration.

B. Synthesis/Layout Integration

Summary: A design flow that limits the number of iterations to converge to a solution in an efficient manner.

Description: It has become clear that the interaction of domains during synthesis can greatly improve the quality of the results. For example, the current efforts to integrate circuit mapping and sizing and layout in the same tool have already produce excellent results. However, further innovations are needed to calculate and optimize routability and ameliorate congestion at the technology independent logic synthesis level when most circuit structures are determined. Additionally, parameterized libraries consisting of partially completed precharacterized cells should also be explored which will require P&R tools which can optimize such cells. Further research is also needed in the areas of regularity extraction and structured layout techniques.

As manufacturing variations become increasingly dominant, synthesis parameters will behave as random variables and must be addressed as such. Investigation of the use of stochastic optimization should be applied here.

Also, in further exploration of synthesis, combining transistor level synthesis (circuit family exploration) with automatic cell and layout generation to automate a pseudo custom design process. For the combined logic and physical synthesis flow to be effective, further explorations at the synthesis and layout level simultaneously that preserve the locality of changes in one description (say logic) when translated into the layout level and affect incrementally the perturbation at this level are of high importance.

C. Power Distribution Design and Analysis

Summary: A power grid solution that provides for the unique power delivery and dissipation requirements across the chip while ensuring reliability concerns are addressed.

Description: Power Grid design algorithms are needed that optimize for noise, power delivery at the module level, and are integrated within P&R. Additionally, these algorithms must rely on accurate models of power utilization (i.e., AF, peak power estimation, etc.) by the different modules it feeds. Research is needed for power distribution optimization in the presence of inductance, and various isolation and decoupling methodologies. Co-optimization of power distribution network with signal distribution needs (clock nets, critical global nets), package design needs, and manufacturing variability needs must also be included (along with a better understanding of the tradeoffs between power grid design and system performance at early stages of design). Algorithms for extraction and analysis will be needed to complete the design process and iterate efficiently to a solution. Quality and Reliability issues (EM) must be comprehended and addressed. Finally, solutions must contain the ability to turn off different portions of the chip for addressing static power dissipation.

D. High Level Planning and Estimation

Summary: Front end design tools that provide tradeoffs and feedback on architectural decisions with respect to area, power, and performance. Should be able to operate top down or bottoms up and handle the multi-terrain dies of the future.

Description: Floorplanning algorithms that consider wire planning and handling, latency planning, with robust physical modeling are of high interest. These algorithms should support partitioning of a design into soft macros taking advantage of special technology features such as multiple Vdd and multi-Vt cells and multi-terrain layout these create. Floorplanning should also comprehend I/O planning (including package). The objective is reduction of power via multiple Vdd and multi-Vt devices, die size optimization with multi-terrain features, potential noise and

coupling violations, and mitigating congestion subject to meeting signal integrity and cycle time constraints. Early floorplanning should also take into consideration the package, thermal, and DFM issues. Subsequent analysis and simulation should include all these constraints. Finally, with the advent of SOC, analog and mixed signal IP Block placement and isolation must be comprehended. FP algorithms that can parse RTL level coding for optimal interface and blocking would be useful. This would require the comprehension of local vs. global interconnect at that level.

For high level estimation, we envision algorithms integrated in one tool that can analyze the behavioral, logical and physical aspects of a design simultaneously and optimize it for area, delay, signal integrity and power. We also need the ability to predict physical, electrical, and performance metrics of a block without implementing a synthesis and layout step. For this to become a reality, suitable abstractions and data models need to be developed. These abstractions need to be able to combine behavioral, logical and physical information efficiently. Any research exploration into integrated data models and physical synthesis should include consistent metrics across various stages of the design/verification flow and algorithms which can optimize across domains.

E. Clocking Design and Analysis above 15GHz

Summary: Clocking solution which supports chip operation above 15GHz.

Description: Conventional clocking methodologies will break down as designs break the 10's of GHz range. Conventional synchronous clocking methods consume too much power and with continued scaling and increasing frequencies, reliability concerns(i.e. excessive skew, jitter, and shape degradation) will become more prevalent. Hybrid synch/asynch schemes and other alternatives to synchronous clocking to address the global clocking reliability issues are of interest. Synthesis of a clock tree based on prescribed skews at the latches enabling cycle stealing techniques and possibly power reduction could be explored. Algorithms should comprehend process and manufacturing variations and should contain ECO capability.

F. Interconnect synthesis and analysis

Summary: Intra-chip communication solutions that address the increasing global and local clock frequencies.

Description: This research will require algorithms that comprehend gate sizing, wire sizing, inverter-pair insertion and placement (both clock and signal), signal routing, global and local interconnect structures, signal integrity (isolation for critical digital and analog signals), and cell place and route simultaneously. These algorithms should understand the special handling of differential signals including coupling and congestion. Bus structures which possess unique characteristics(i.e. Xcap and mutual inductance) must be understood. Additionally, the ability to perform true simultaneous synthesis of multiple interconnects (as opposed to net ordering) and comprehend routing layer assignment as well as shielding. In addition to accurately modeling the unique characteristics of each layer, there is a need for variable accuracy, on-the-fly RLC extraction and analysis (model to be lumped or distributed depending on frequency) to incorporate the impact of the wire design on noise and timing. Further research in frequency dependent Model Order reduction for multiple signals in the distributed RLC domain are needed.

G. Timing analysis and verification

Summary: Efficient and accurate timing analysis solutions in the presence of emerging circuit families, process technologies (including SOI), and manufacturing variations.

Description: Timing analysis accuracy in the presence of process and statistical variations (power grid variations, temperature, noise). This analysis should consider logic correlations for implementing false path analysis as well as consider multiple input switching. This effort must include incremental analysis to address the issue of productivity and timely processing. Accurate layout modeling (layer considerations) and estimation must be comprehended when considering the interconnect portion of the delay. Timing analysis must comprehend hybrid synchronous/asynchronous clocking schemes and allow easy verification of the asynchronous interfaces involved.

For Analog design, timing analysis/verification during and after layout phases in the design cycle is challenging, as the timing characteristics of the analog blocks have to be accounted to enable chip or block-level timing verification, which can be both static and dynamic. Improved timing analysis algorithms are also required for designs based on SOI technologies; such algorithms will comprehend the variation in the delay of a device based on its switching history.

Additionally, timing analysis of high performance SOC circuits requires capturing the time scales of all circuit types in the design purposes. One time scale is equivalent to real world time, where events happen on the millisecond scale. The other is the internal clock rate of the circuit, which is where events happen on the nanosecond scale. Simulating correct behavior of such circuits during events such as powerup requires extraordinarily large numbers of clock cycles and a 'smarter' timing engine.

Finally, this research should comprehend the effect of multiple noise sources, including substrate and crosstalk, as well as NBTI (negative bias temperature instability).

H. Research Directions in Correct by Construction Design

Summary: Circuit, synthesis and layout solutions to enable predictable correct-by-construction design that enhances productivity by avoiding onion-peeling iterations.

Description: Traditional CAD research has focused on iterating between optimization and analysis/verification at each stage of the design process. However, this paradigm does not scale well to very large designs at multi-gigahertz frequencies, since the micro-engineering of each device, wire and path becomes prohibitively expensive in such designs. Furthermore, local optimizations required to fix failing devices/paths often create new problems elsewhere in the design, resulting in numerous iterations before convergence is achieved. Instead, solutions are needed to the traditional circuit design, synthesis and layout problems that enable predictable "correct-by-construction" design (even if it is not fully optimized) that requires little analysis/verification overhead and few onion-peeling iterations. In an effort to enhance productivity, these solutions will break the optimization-verification loop by designing to specs (rather than for optimality), trading off some of the optimality for design techniques that result in predictable, guaranteed correct designs.

I. Design and Verification of mixed signal designs

Summary: Solution for mixed signal designs where interaction with digital circuits on chip is comprehended.

Description: Verification of mixed signal design continues to be a big challenge due to poor understanding of the interactions and requirements of digital and analog interfaces ; Analog design constraints, like noise awareness - substrate coupling, parasitic interaction etc. - need to be incorporated in digital design tools for timing, placement, and routing to enable designs of reasonable complexity.

J. Design for embedded System On Chip

Summary: Solutions that address the physical design needs of large, complex SoC designs.

Description: Current systems-on-chip (SoCs) are complex devices used primarily in embedded systems. SoC designs typically contain one or more embedded cores (DSP or microprocessor), embedded memory, specialized and peripherals logic, and often analog/mixed-signal components. SoCs are often built by assembling existing cores or IP blocks (IP reuse) and adding (synthesizing) proprietary logic and software. SoC design spans a range of problems, including: core selection, system performance analysis and IP verification, IP block reuse (hard IP reuse or soft IP reuse), floorplanning and global SoC chip integration, SoC design data management and layout for large designs, and mixed-block timing analysis. While many SoC design problems are shared with microprocessor and ASIC design styles, SoCs have distinct characteristics: the sheer size of SoCs, the diversity of components in an SoC, a design style that incorporates extensive design reuse (often hard IP reuse), and the nature of the target embedded systems (which are often cost and time-to-market driven). In an embedded SoC, different domain types (logic/memory,

digital/analog) may interact heavily, thus complicating possible optimizations. The problem is made yet more challenging because of the gray/black box nature of several of the IP blocks on the chip, which requires different approaches for IP verification and timing characterization and analysis.

New research needs to be developed to address the specific needs of SoC in the physical design arena, as there are few tools, flows and techniques that are specialized to aid the design of complex SoCs. The research needs include: Floorplanning and chip integration algorithms for SoC designs (see problem D); timing analysis supporting mixed types of circuits (see problem G); algorithms and techniques to support IP reuse, characterization and verification for SoCs; data management and frameworks to support large and complex SoC chip design and integration.

K. Optimization and Analysis for Power

Power is becoming a dominant factor in many designs, where sacrifices to timing or area performance may need to be made in order to deliver silicon which meets power requirements as driven by packaging or customer application. Techniques need to be developed where power is the dominant optimization target, with timing and area secondary requirements. We expect that all algorithmic solutions to the above listed research areas should include methodologies to reduce dynamic and leakage power at all points in the design flow. This includes synthesis (see section B), place and route (see section A), and during timing analysis where reduction of gate size for non-critical paths should be implemented. In summary, power reduction and management should be part of the objective function during all optimizations.

Additionally, because today's SOC designs may contain collections of both digital and analog IP, the analysis/optimization techniques must apply to hierarchical designs. They must also recognize the power characteristics of analog design, which are not based on clock rates. Characterization and modeling for power must be available for IP cores to improve efficiency of power analysis. Algorithms are needed for high level power estimation and early estimation that might consider physical design effects (see section D).

Some known design techniques for power reduction include gated or skewed clock, asynchronous design, multiple-Vt, and multiple or variable VDD implementations. These and other design techniques must be comprehended and supported in the physical design phase, with analysis and optimization capabilities. Synthesis for low power logic families (sub-threshold based circuit design) should be supported.

Finally, physical design tools must comprehend power density issues and their resulting thermal effects (see section A). Going forward, physical design must support future methodologies in power management.

Footnotes:

1) Manufacturabilty, though only listed explicitly in some problem statements, needs to be considered within all areas and which may imply the use of statistical methods to support this effort.

2) CAD research is intended ultimately to provide design productivity improvements. This includes fast algorithms / data structures for early design phases for timing and layout parasitics. All research above should cover faster algorithms and data structure in Logic/PD/PV which support full analysis or incremental ECO analysis (e.g., to drive the engine of VLSI timing driven tools). Also, better data visualizations/reporting to aid design trouble shooting in layout congestions, timing speed paths, onion peelings, are needed.

IV. Further refining the needs of SRC member companies

The above listed needs for industry describe a complete solution in the CAD areas of synthesis, physical design, and timing analysis & verification for aiding the design engineer. However, we recognize that a portion of these needs may be met outside of academic circles (i.e., semiconductor company in-house research as well as solutions from EDA). We therefore further refine the list to include those areas that we feel are best served by research within academia due to these above factors. Again, though not specifically mentioned, we believe that manufacturabilty as well as power reduction and management should be considered as part of any objective function during all optimizations. Full analysis or incremental ECO analysis should also be addressed.

A. Placement and Routing:

Description: Keen interest in the solution for placement of thousands of large blocks and millions of small blocks in a reasonable time while considering lithographic techniques such as OPC and PSM which impose additional constraints on the layout. Additionally, placement algorithms that create a more even thermal profile are of high interest as power density will become a reliability issue in the near future. Placement algorithms that comprehend the unique requirements of analog circuits as well as SOC intra-die circuit family interactions are also of interest.

B. Synthesis and Layout Integration:

Description: Optimizations focused on routability and congestion at the technology independent logic synthesis level. Parameterized libraries consisting of partially completed precharacterized cells that can be optimized by place and route tools in these situations. Exploration of synthesis methodologies that provide for the automation of a pseudo custom design process.

C. Power Distribution Design and Analysis:

Description: Co-optimization of power distribution network where signal distribution (clock nets, critical global nets), package design, and manufacturing variability along with a comprehending power grid decisions and their impact on system performance at early stages of design. Power Grid design algorithms that comprehend inductance and various isolation and decoupling methodologies and which optimize for noise, power delivery at the module level, and can be integrated into P&R.

D. High Level Planning and Estimation:

Description: Algorithms that analyze behavioral, logical and physical aspects of a design simultaneously and optimize it for area, delay, signal integrity and power. We encourage the exploration of integrated data models and physical synthesis and consistent metrics across various stages of the design/verification flow.

Floorplanning algorithms that consider wire planning and handling, latency planning, and robust physical modeling. They should also take into consideration package, thermal, and DFM issues. Subsequent analysis and simulation should include all these constraints. Finally, with advent of SOC, analog and mixed signal IP Block placement and isolation must be comprehended.

E. Clocking Design and Analysis above 15GHz:

Description: Synthesis of a clock tree based on prescribed skews at the latches enabling cycle stealing techniques and possibly power reduction could be explored. Algorithms should comprehend process and manufacturing variations and should contain ECO capability. Alternative solutions to a globally synchronous methodology to address reliability issues are welcome.

F. Interconnect Synthesis and Analysis:

Description: Exploration of bus structure characteristics and topologies. Explore true simultaneous synthesis of multiple interconnects(as opposed to net ordering). Variable accuracy, on-the-fly RLC extraction and analysis(model to be lumped or distributed depending on frequency) to incorporate the impact of the wire design on noise and timing is of interest.

G. Timing Analysis and Verification:
Description: Timing analysis accuracy in the presence of process and statistical variations(power grid variations, temperature, noise) and input switching. Analog design, timing analysis/verification during and after layout phases.

H. Design and Verification of Mixed Signal Designs: See section IV

I. Research Directions in Correct by Construction Design: See section IV.

J. Design for embedded systems on chip:
Description: New research needs to be developed to address the specific needs of SoC in the physical design arena, as there are few tools, flows and techniques that are specialized to aid the design of complex SoCs. The research needs include: Floorplanning and chip integration algorithms for SoC designs (see problem D); timing analysis supporting mixed types of circuits (see problem G); algorithms and techniques to support IP reuse, characterization and verification for SoCs; data management and frameworks to support large and complex SoC chip design and integration.

K. Power analysis and optimization:
Description: Specific research areas for academia include hierarchical power-driven physical design for mixed-signal design, physical design for circuits using low-power design techniques (gated or skewed clock, asynchronous design, multiple-Vt, multiple or variable VDD, et. al.), and power analysis with thermal factor considerations.

V. Technical Contributors:

Many thanks to the effort put in by the SRC PD Task Force in creating this document. Task Force members are listed below:

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