Semiconductor Research Corporation

Computer Aided Design and Test Sciences

Research Needs in Test and Testability

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Overview

A committee of Test experts from SRC member companies have identified research needs in test and testability which are not adequately addressed in the current SRC portfolio. Current and near-future semiconductor products will increasingly be implemented as Systems on a Chip (SoC), giving rise to new and difficult test challenges. Testing of analog functions in general has not historically been automated to same the degree as digital testing. Embedding of analog functions deep within largely-digital SoCs compounds the difficulty; now, in addition to the traditional issues of signal generation, precision measurements, etc., we are faced with major problems in test access, noise and coupling to adjacent circuitry, and signal analysis. The success of scan-based test methods in managing the complexity of testing large digital chips, along with the increasing difficulty of creating broadside tests for application by expensive high speed testers, requires that on-chip test hardware (e.g. scan or BIST) will be used for an increasing portion of at-speed testing. The nature of high speed circuit design techniques, along with the extra detail required by more complex fault models, presents several new problems to traditional DFT and ATPG approaches. With digital ASIC clock frequencies already in excess of 1GHz, testing for defects that affect signal integrity is becoming critical. While designers attempt to avoid crosstalk and noise problems through conservative design practices, present-day design tools cannot assure that all circuits will function properly over all manufacturing variations. Advanced testing techniques will be needed both to confirm design practices and to identify circuits which fail due to timing and crosstalk issues resulting from manufacturing variability. The concerns during testing are accurate speed characterization, establishing frequency shmoo holes (a circuit containing races often works on some frequency bands and not necessarily at all frequencies at or below maximum), and ensuring logical correctness in the established frequency bands.

The above discussion highlights some of the most pressing concerns identified by the SRC Test Committee, but is by no means exhaustive. Many challenges remain in more traditional areas of Design for Testability, Built in Self Test, Diagnosis, Automatic Test Pattern Generation, etc. The

following sections enumerate some specific areas of interest for new research in the highest priority areas.

1. Mixed Signal/Analog Test and Testability

(a) Fault models, defect models, and measurement methods to discriminate good vs. bad circuits for analog and mixed-signal circuits.

(b) Test metrics (fault/defect coverage and measurement precision) required to provide the quantification needed to define relative quality evaluation for mixed-signal test.

(c) Technical and economic trade-offs between additional analog/mixed-signal tester instrumentation vs. built-in circuit testing methods.

(d) Test methods for analog and mixed signal circuit families which utilize the logic testers employed for most SoC chip testing today.

(e) Automatic determination of the boundary between the analog and digital circuits and inserting appropriate test observe and control points for both portions.

(f) Built-in self-test and design-for-test techniques for analog/mixed signal.

(g) RF subsystem testing, test access, defect models

(h) Test methods for embedded analog blocks in largely digital SoCs: PLL, ADC, DAC, etc.

2. At Speed/AC Testing

(a) Understanding and characterization of DSM physical defects that may warrant at-speed/AC testing

(b) Development of surrogate fault models that facilitate easy automatic test development for large ICs without sacrificing the coverage of the underlying defects

(c) Practical scan based delay fault test development and test deployment techniques for large ICs

(d) Techniques for power and noise management during at-speed testing, including limiting power dissipation and managing noise during scan testing or BIST

(e) Test development methodologies and tools for large ICs with non-homogeneous design and testability characteristic (for example, SoCs).

(f) Development of "Speed Predictor" circuits and speed co-relation techniques for speed binning of ICs early in manufacturing

(g) Development of practical surrogate testing methods that provide coverage of defects covered by at-speed testing and AC parametric testing without actually testing at full speed

(h) Development of suitable DFT and testing methods that reduce or eliminate the

dependence on high performance, highly accurate testers, including designing appropriate on-chip testability hardware (e.g., scan or BIST)

(i) Re-architecting of the test resources on chip, test fixtures and testers that provide at-speed and AC parametric coverage with lower overall cost for several generations of DSM (Test resources partitioning),

(j) Testing of high performance circuit types, e.g. dynamic, self-timed, and asynchronous circuits

(k) Designing appropriate on-chip testability hardware (e.g. Scan or BIST)

(l) Incorporating accurate timing into test generation models

(m) Testing across multiple clock domains

(n) Diagnosis/debug techniques to address AC scan test static and dynamic failures

3. Signal Integrity Test

(a) Accurate speed characterization,

(b) Establishing frequency shmoo holes (a circuit containing races often works on some frequency bands and not necessarily at all frequencies at or below maximum)

(c) Ensuring logical correctness in the established frequency bands.

(d) Test development and coverage measurement techniques for cross-talk induced noise and delay

(e) Testing for cross talk in a hierarchical design environment with embedded cores

(f) Faults resulting from a combination of ground bounce and crosstalk.

4. Embedded Test for SoC

(a) Embedded testing methods and structures for noise- and coupling-induced faults

(b) Power management during test

(c) Testing of embedded arrays, memory, programmable logic, etc.

(d) Testing reconfigurable and platform-based SoCs

(e) Test methods for interactions between analog and digital subsystems