Research Needs in Test and Testability

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INTRODUCTION

Until recently, the development of tests for circuits has been a stepchild of design – when designers finished a chip or system, they would then hand it over to test specialists, expecting that they could provide whatever tests were needed. Today, for almost all types of circuits and systems, this is a recipe for failure. None of the three goals for a successful design and manufacturing startup cycle will be met – the time to volume production will miss the market, the quality of the design will fail in performance or reliability, and the cost as a function of yield will exceed what the customer is willing to pay. Only by involving test planning and test development in all phases of design and manufacturing startup can a design be successful.

Many factors contribute to this added complexity, in addition to the well-known effects of shortening time-to-market requirements and Moore's Law effects of higher densities and more complex devices. Frequencies of operation and clock rates reach into ranges once considered the domain of electromagnetic wave analysis and microwave plumbing. Below 100 nanometers, manufacturing lithography requirements of optical phase correction alter the mask layouts themselves, introducing patterns which affect both performance and testability – no longer can probe pads be added after design completion or probe parasitics be neglected

The sections below analyze the test needs of specific types of circuits – analog, digital, mixed-signal, RF, etc. But "test" is two-dimensional. For circuits there are several types of tests – each unique in its requirements and each facing challenges today. ***Research proposals responding to this document will be required to identify which category(ies) of testing are addressed by the proposed research.***

  I. Characterization testing: Testing to prove that performance meets design goals, to establish ranges of successful operation and to troubleshoot failing devices. Devices can be moved between test equipment, speed is less important than accuracy, number of devices to be tested is low, data collection and analysis features are important.
 II. Wafer probing: Testing done before the manufactured wafer is diced into individual chips. Since package costs often exceed chip costs, this is done to reject devices that will fail in final test. Challenges in probe testing are that contact to the chip pads is by spring-loaded needles, that it must be rapid, and that it must be highly predictive of final test yield without the ability to run some tests possible only on packed devices. Sometimes, advantage can be taken of

access to internal structures such as probe pads that are not accessible after packaging. Multiple probing, using different test equipment, is possible but adds significantly to cost. Equipment is expensive; its depreciation cost cannot be neglected

III. Final testing: Testing packaged devices. "Fail-safe" testing is a requirement – shipping bad devices to a customer can be commercially disastrous, yet rejecting good devices adds major cost penalties. Binning devices is often required, to allow shipment to less-demanding (and lower price) applications. It shares many requirements with wafer probing – need for speed, penalty for multiple test stations, extremely high cost of equipment. It has the advantage of better connections to device under test, but no longer has access to internal test points.

IV. Reliability screening: A collection of stressing and testing techniques to weed out devices that can fail in use. It uses high temperatures, high voltages, and "shake-and-bake" environments to accelerate and detect incipient failures. Very expensive; it will be eliminated where possible

V. Field testing: Once shipped and even assembled in a final system, a device may still need to be tested. Mission-critical applications may require in-situ testing. Maintenance costs to identify defective components are very high. The sophisticated, costly equipment available during design and manufacture is seldom available in the field. Here, self-diagnostic and BIST (Built-In-Self-Test) features can perform double duty – reducing the cost of manufacturing and facilitating successful life in the field.

VI. Failure Analysis and Diagnosis: When failed products are returned from the field by customers, it is important to be able to determine the exact cause of the failure, in order to improve the product and its test procedures in the future. This is typically a slow, expensive process, but will continue to be critical into the foreseeable future in order to maintain product quality and customer confidence.

Acknowledgements

In the sections that follow, we outline the major research challenges in all fields of test. While this is not an exhaustive list, it represents the consensus views and priority needs of the SRC community. ***Research proposals responding to this document will be required to identify which specific section(s) are addressed by the proposed research.***

1. Heterogeneous Systems-on-a-Chip

1.1. Test development methodologies and tools for large ICs with non-homogeneous design and testability characteristics.

There are well-defined methods for testing homogeneous (purely digital logic) integrated circuits. Advances in the semiconductor industry continue to enable an increasing level of complexity to the point where designers have to integrate large blocks in order to complete the chip productively. The traditional test methods for digital circuits are extensible, but only to a certain point. The convergence of complex blocks, which may be heterogeneous in nature, is starting to challenge current test methods. New design flows for SoCs may include heterogeneous blocks of intellectual property designed by multiple sources. These blocks can usually be validated and tested individually using traditional methods, but these techniques do not always apply when testing the full chip. The provider of a block of IP must use techniques that facilitate testing at the full chip level. The top level of the design must also allow enough controllability and observability to enable any BIST included with the IP.   There are no fixed guidelines or standards for IP providers at the time of this publication. As these guidelines emerge, we need to consider facilitating techniques for efficient testing during production.

1.2. Power dissipation and noise in test mode

Heterogeneous SoCs introduce a new class of issues for production testing. A chip operating in test mode does not always exhibit the same characteristics as it does during normal operation. Power dissipation, for example, may be much higher than normal if multiple blocks are targeted simultaneously to decrease test time. Increased power dissipation may cause an increase in temperature, voltage drop, and possibly cross talk, among other effects, far beyond the requirements necessary under normal chip operation. The design guidelines for typical operation may not be adequate to support such conditions and cause an operational unit to fail during test mode.

Power and noise management during test is critical for successful application of BIST, scan-based at-speed tests and SOC tests. Design, test scheduling and test vector generation techniques to manage power and noise during test must be devised.

1.3. New fault models for deep submicron systems on chip

The emergence of SoCs is also forcing designers to use new process technologies for higher performance. These new technologies may also introduce new issues during test. Traditional techniques, such as I_{DDq}, may not be applicable in other technologies. Fabrication using new materials may exhibit new defect mechanisms that are not modeled using the traditional stuck-at fault models. New test methods and fault models must be developed to address these situations.

1.4. Advanced test equipment

The development of test equipment will also face obstacles. New process technologies accelerate the obsolescence of test equipment. SoC designs will require an increasing number of I/Os operating at higher speeds and with reduced parasitic requirements. High-speed digital designs

may exhibit characteristics and present issues that were traditionally observed only on analog designs. Designs may be more sensitive to conditions such as jitter, placing a requirement on the analysis instrumentation. Test equipment must measure parameters without degrading circuit performance. Digital circuit testers can compensate presently for some degradation using an ideal time delay model and subtracting an error term. Degradation introduced when testing analog circuits to parameters such as bandwidth, slew rate, and jitter, is far more complicated to control, and, at the time of this publication, there are no generic solutions to compensate for them. In general, much research effort will be required in order to find effective solutions to keep the cost of test under control.

1.5. Testing reconfigurable systems on chip

Reconfigurability adds a new degree of freedom to SoC architectures, requiring a significant paradigm shift away from traditional test methodologies. The new degree of freedom comes at the expense of increased complexity but with the potential advantages of meeting low power constraints while maintaining increased performance. Reconfigurable architectures are heterogeneous systems that typically take advantage of switched data and RF paths, employ adaptive signal processing algorithms, or use reconfigurable logic to implement state machines. Given the heterogeneous nature of these architectures, testing techniques for reconfigurable SoCs must address the same issues stated in Section 1.1. The concept of reconfigurability will give rise to new test methodologies such as reconfiguration logic reused for testing circuitry or other control flow monitoring. In general, the testing methodologies developed for reconfigurable SoCs must follow the same flexibility that reconfigurable architectures permit.

2. Digital System Test

2.1. RTL testability analysis

The traditional method of inserting testability enhancements has been at the gate level. However, in the "RTL-to-Placed-Gates" or "RTL-to-GDS2" synthesis methodologies, insertion of testability enhancements at the gate level is impossible (or at least highly impractical). Furthermore, any enhancements made at the gate level would not be reflected in the RTL. RTL level testability analysis tools are required, which can identify areas of RTL that can create test coverage issues and suggest fixes, so that 99.95% test coverage is achieved despite lack of access to gate level information.

2.2. Techniques for on-line test/fault tolerance

Miniature dimensions, complex processes and sheer number of elements lead to a situation where it may no longer be realistic to manufacture chips that are fault-free upon manufacturing and throughout their lifetimes. As a result, practical methods much be developed for fault tolerance for portions of ICs beyond memory. In addition, the need to tolerate reliability-type fails drives a need for on-line test methods as well.

2.3. Clock testing

Standardized techniques are needed for determining "clock-data" timing on different protocols (clock extraction, deterministic/random jitter, wander etc.) and clock jitter analysis techniques in high volume manufacturing.

2.4. Speed-Related Testing Issues

Design for testability and testing methods that reduce or eliminate the dependence on expensive, high-performance, highly accurate testers are urgently needed. These methods should achieve high defect coverage without significantly increasing test times or test data volume (preferably reducing test costs over time). The following items are examples of important needs in this area; research is needed to define and develop advanced on-chip design-for-test (DFT) features as well as external test methodologies.

Surrogate methods
Practical surrogate testing methods that provide coverage of defects covered by at-speed testing and AC parametric testing without testing at full speed through the tester/IC interface. These methods should not require high-speed testers—but may use DFT methods that generate high-speed signals within the IC. Development of surrogate fault models that facilitate automated test development for large ICs without sacrificing the coverage of underlying defects.

Scan based methods
Practical scan-based delay fault test development and test deployment techniques for large ICs. These methods should have no significant impact to product time-to-market—requiring little debug or customization effort for a particular design.

Testing of high performance circuit types
Dynamic, self-timed, and asynchronous circuits, thorough speed-related testing for ICs with multiple clock domains.

Pattern reduction
Efficient pattern reduction methods that enable cost effective defect screening while achieving very high quality levels. Ideal methods would reduce the cost of test.

Defect models
Understanding and characterization of deep sub-micron (DSM) physical defects that may warrant speed-related testing.

Debugging and diagnostics
Diagnostics/debug techniques to address AC scan test static and dynamic failures.

Diagnostic methods for ICs with logic BIST
Such methods may require high-speed data collection and off-tester analysis of LBIST data.

Crosstalk induced noise and delay

Test development and coverage measurement techniques for cross-talk induced noise and delay. Faults resulting from a combination of ground bounce and crosstalk

2.5. BIST for systems-in-package

The best approach for systems-in-package (containing ASIC and memory) testing is to use memory BIST built in the ASIC to test the memory chips in the SiP that are external to the ASIC. This requires test simulation/generation tools that can incorporate the SiP parasitics and memory functional models (e.g. Verilog representation with timing attributes). The diagnostic capability of the memory BIST is also important. It is necessary to be able to identify the failing memory chip and the failing memory addresses.

2.6. Eliminating burn-in

Burn-in has historically been the most effective method of screening parts that are susceptible to infant mortality. However, as progress is made in defect based test methods, it has been observed that these new test methods are capable of reducing the infant mortality rate and reducing or eliminating the need for burn-in. While defect based test shows promise in this area, a full understanding of the impact of these methods is not yet at hand. In particular, research is needed to quantify the early failure rate reduction, the overkill and the cost of these test methods. In addition, work should be focused on maintaining the effectiveness of traditional defect screens such as I_{DDq} and the development of new defect screens that can reduce the need for burn-in.

3. Analog Test

This section discusses test needs for analog ICs that do not perform RF functions – a separate RF section lists needs beyond traditionally analog functions for RF circuits. A separate Mixed Signal section treats needs where the digital circuitry adds test needs to the analog blocks such as noise injection or where using available digital test equipment to perform analog tests would simplify wafer probe or final testing.

3.1.   BIST and DFT techniques

It is difficult to test complex analog functions with external test equipment, particularly in wafer probe and final test. The connections, leads and switches add parasitics and limit frequencies and accuracy, and the equipment is complex and expensive. Can BIST (built-in-self-test) and DFT (design-for-test) substitute? ADCs, DACs, signal sources, threshold detectors – these are often already available on chip or can be added at acceptable cost. What types of analog circuits lend themselves to BIST and DFT techniques? What innovative BIST and DFT techniques can be developed? An additional payoff for successful BIST deployment is its availability for field testing – how could this be facilitated?

3.2.   BIST for analog circuitry embedded in largely digital and SiPs

Where significant digital functionality is available on the chip or in the package, BIST can make use of it. Microprocessors and their associated components can generate signals, set up paths, trigger measurements and provide a variety of other functions. How can this be applied to each of the many types of analog circuitry which may be on the same chip - PLLs, ADCs, DACs, oscillators, amplifiers, ...?

3.3.   Fault/defect modeling

Developing efficient tests to screen out faulty circuits at either wafer probe or final test can be facilitated by accurate, detailed models of how particular circuits fail. It is often difficult, even impossible, to perform functional tests of complex analog blocks in manufacturing. Structural tests that show that no structural defects are present can often be more easily and accurately performed. But what defects to test for, and how they can be practically tested in a manufacturing environment is the subject of this need for research. Shorts and opens are obvious structural defects, but leakage paths, patterning errors between matched devices, and many others will also produce defective circuitry.

4.   Mixed-Signal Test

The percentage of VLSI and SOC devices containing analog functions, DACs, ADCs, DSPs, etc is on the rise. With the new advancements in multimedia and consumer electronics, these analog components have become an integral part of the chip industry mainstream products. The increased complexity and functionality of products containing Mixed-Signal and analog circuits and the reduced access to internal circuit nodes, makes testing these devices a major challenge. The traditional test strategy for mixed-signal systems relies on functional test, which is expensive, requires long test development and test times, and requires high cost ATE. Given the trend towards very complex systems on chip, functional test is no longer sufficient to provide a high-test quality at a reasonable cost to the vendors and the customers. Mixed-signal and analog systems of interest are those of high packing density where testing of internal nodes in production and in the field is prohibitively difficult.

4.1   DFT and BIST for mixed signal

DFT and BIST techniques for Mixed-Signal designs are needed to alleviate to reduce I/O data rate, enable low pin count testing, reduce the dependence on expensive instruments and provide high quality characterization of internal product specification and overall functionality. It is important to note that a practical DFT/BIST solution should cover most of the previously mentioned needs as well as being non-invasive as much as possible in order not to interfere with the system design. Area overhead, power consumption, performance degradation, additional design efforts are all issues which have prevented the wide acceptance of Analog / Mixed-Signal BIST solution and must be addressed upfront in any proposed solution. An ideal BIST solution is a drop in IP or macro that treats the system under test as a closed black box.

4.2   Embedded analog block testing

Due to the increased percentage of embedded analog blocks in Mixed-Signal designs, the fundamental issues for analog measurements such as measurements precision, measurement sample deviation from measurement mean, measurement with and without stimulus, systematic error, noise, etc, need to be addressed for any high-speed Mixed-Signal solutions.

4.3   Reconfiguration-based self-test methods

Reconfiguration techniques (such as loop around, bypass to gain access to internal nodes, analog checksum, build in sensors) should all be re-examined for performance and effects on high-speed mixed-signal systems.   Existing test techniques such as DSP based self-test, delta-sigma

modulation and pseudo-random testing should also be looked at in light of the above-mentioned high-speed mixed signal considerations and whether they could be used for very high-speed systems. In addition, new combined BIST techniques for high speed analog-mixed-digital systems are very desirable

4.4   Fault models

Fault models for analog and mixed signal circuits can be classified into two categories: catastrophic faults (sometimes called hard faults) and parametric faults (sometimes called soft faults). A catastrophic fault model is analogous to the stuck-at fault model in the digital domain in that the terminals of the component can be stuck-open or stuck-short. Parametric faults, on the other hand, are deviations of component parameters that result in performance out of acceptable limits or no function at all. Since the yield and performance of analog/mixed-signal chips are heavily tied to parametric faults, and since current sub-micron process technology has induced several new invisible faults (statistical process variation, mismatch, particles blocking implant, cross talk, substrate noise, etc.) which could alter analog /mixed-signal device performance, investigation of new fault models covering the above effects could provide great value to our challenges. Macromodeling and fault macromodeling techniques for analog components, hierarchical fault simulation, efficient fault simulation methodology and techniques, and deterministic test generation techniques for DC and AC stimuli should be investigated to improve our Mixed-Signal test capabilities. However, any new models should be correlated to realistic statistical process, device and primitive cell parameters to be of any practical value. These models should also be easily implementable in existing industry standards platforms, *e.g.* OpenAccess. Stand-alone solutions will have diminishing value when it comes to industry use.

5.   RF Test

Currently, the industry is facing serious problems regarding RF measurements beyond 2.5 - 5 GHz. It is very expensive to test parts in excess of 2.5 - 5 GHz at wafer level or package tests; special testers or added hardware modules are needed to perform such tests, with added cost and test time. Designs at 10 GHz and beyond are currently being developed, but there are no production testers capable of testing at those frequencies. It is imperative that new techniques be developed which allow high-frequency mixed-signal circuitry (1-30 GHz) to be fully tested and characterized for complex test specifications using low-cost testers.

5.1   Built-in test for RF

On-chip built-in test (BIT) for RF systems using low cost external tester support is a very attractive solution. Built-In Test involves designing high-speed/RF test hardware on-chip, supporting the test hardware with design-for testability features and designing in standard communication protocols that allow an external tester to control the test procedure with low bandwidth access and hence, lower cost external testers. In products with on-chip DSP, almost all the test functions can be performed on-chip, transforming the built-in test (BIT) into autonomous built-in self-test (BIST) with little external tester control. A final note here is in order; RF and High-speed system designers have always resisted any embedded circuits, which could interfere with the operation and performance of their designs. Their reasons are valid and have been published; therefore current BIST methodologies may not fit very well in RF or high-speed products. Therefore the emphasis should be on developing new methods with great consideration for the sensitivity of the RF circuits

to any modification or externally embedded circuits; ideally, any new method should look into non-invasive solutions.

5.2   Noise and crosstalk testing

To make matters more difficult, new SOC products are integrating Mixed Signal and RF on one chip. One of the most difficult problems these products face is noise and cross talk. Also, as the number of fast switching transistors increases, so does the power supply noise. For these new classes of products and for high speed Analog/ Mixed Signal chips in general, new methods to analyze, isolate and measure the effect of noise and cross talk in the RF domain are needed. Some attention should also be paid to consider what some have reported in the industry of the coupling and integration of cross talk and noise sources in the RF frequency domain.

6.   *Model and Constraint Extraction*

This section discusses test needs in the area of Gate Level Model Extraction from Transistor Level Schematics. High performance designs often rely on custom or semi-custom design methodologies centered on design and circuit optimization at the transistor level. A cell or mega-cell in such designs is a manually manageable piece of design that stands on multiple views. Each view is created to support a level of abstraction suitable for a particular analysis. Examples include a transistor schematic view for circuit simulation, timing characterization and noise analysis; a gate level schematic view for verification, fault simulation, automatic test pattern generation; a physical view for placement and routing; RTL view for high level specification and simulation and so on. A gate level schematic view of a cell is necessary for supporting test related tasks such as fault simulation and automatic test pattern generation. There is some literature on extraction of gate level models from transistor level schematics. However, their reach does not stretch far beyond combinational gates.

6.1   Extracting complex functions

Research on extraction techniques for complex functions such as multi-ported latches, Random Access Memories, Content Addressable Memories is needed to automate the process and boost design productivity.

6.2   Constraint extraction

With structural test techniques (for example: scan), a design often has multiple modes of operation such as functional mode, scan mode, direct access mode etc. Many transistor level schematics are designed with certain assumptions about their intended use. Such as, a fully decoded MUX may be designed with the assumption that the select inputs are one hot, i.e., one and only one input can have a logic value 1 and all others must be at logic value 0. While this may certainly be a valid assumption in functional mode, such an assumption may be invalid in a different mode. For example, in scan mode if all select inputs of the said MUX come from scan elements, such conditions may be violated during scan. To avoid illegal states and contention between power supply nodes, "constraints" on values are placed on a gate level model. Since most such constraints are visible at transistor schematic level, an automatic gate extractor should also extract such constraints and place them on gate level model. Once again, research in this area can help eliminate "illegal" scan vectors and improve correctness of test vectors and design productivity.