

SRC Needs Document

Logic, Physical, and Electrical Design and Analysis Tools

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Research needs in design tools are driven by both constant and changing factors in the design and development of integrated circuits. Constant factors are driven by the industry's desire to reduce cost while creating more valuable end-user products based on innovative circuits and systems. These factors include:

- Minimizing manufacturing cost by increasing yield and reducing die area and test cost.
- Integrating more transistors and diverse logic types on a single chip, to increase system capability and drive total system cost down.
- Attaining the best chip and system performance within a specific power envelope, in particular maximizing computing speed while minimizing both static and dynamic power.
- Improving system quality and reliability.
- Reducing the time-to-market and total design cost for new designs, for incremental redesigns, and for designs ported from one technology node to another.

As lithography improves along Moore's law path, new opportunities for higher performance, greater integration, lower cost, etc. are weighed against design and manufacturing challenges at these new densities. These new opportunities and leverage points for improved circuit and system design create changing sets of possible techniques and technologies for design, influencing CAD research needs. Changing factors influencing current physical design CAD research include (but are not limited to):

- Sub-wavelength lithography and resolution enhancement techniques.
- Integration, including embedded DRAM, mixed-signal, system-on-chip (SoC) design and system-in-package (SiP) design.
- Interconnect dominating global DSM delays, SOI, advanced clocking techniques, etc.
- System level design for reduced power, increased reliability, and robustness to process variations.
- Tighter integration of physical design and synthesis.

However, beyond improving the analysis and synthesis in current flows, there is an opportunity to revisit the design flow organization itself. For example, old flow paradigms that separated timing and synthesis from layout have broken down at technology levels where the details of the implementation impact systematic within-die variations, and where interconnect dominates timing and power. Needed are new design paradigms and flows that address these new designs without requiring excessive designer effort. This may take the form of algorithms with multi-objective functions which allow early prediction of the impact of implementation on design performance, out-of-sequence optimization of the design at any point in the flow, and the integration of layout and synthesis and correct-by-construction methods where layout restrictions and layout uniformity targets are driven from higher levels. Research is needed, not that incrementally improves existing approaches, but that alters the landscape and provides significant leverage to designers working three to five years from now.

This document is designed to encourage submission of research white papers and proposals from universities for consideration by SRC member companies in the design tools area of the SRC's Computer-Aided Design and Test science area, which covers all CAD tool areas except test and verification. Note that though they are specifically called out here for emphasis, tools addressing mixed-signal design, system-on-chip and system-in-package design, and memory

design, as well as digital design, are sought in all topic areas. Submitters should indicate a primary area in which their white paper should be considered, and may submit one or two secondary areas. Note that in addition to outlining and addressing a problem in one of these areas, indication of present or planned interactions with engineers and researchers from SRC member companies is specifically encouraged.

1. Power Management and Analysis Tools

- a. Leakage power management
- b. System-level power prediction and management
- c. Synthesis and physical design techniques using low power circuits
- d. Tools addressing power/thermal considerations

Power is the dominant factor in many designs. Approaches are needed to reduce dynamic and leakage power at all points in the design flow, including design planning, synthesis, place and route, and performance analysis. Power reduction and management need to be part of the objective function during all optimizations. Analysis and optimization techniques are needed for hierarchical design, for analog and mixed signal designs, and for SiP or SoC designs using heterogeneous cores. Algorithms are needed for high-level power estimation and synthesis for low power logic families. Physical design tools must comprehend power density issues and their resulting thermal effects.

2. Timing Analysis and Optimization

- a. Timing analysis in the presence of manufacturing variations
- b. Timing analysis for emerging CMOS technologies
- c. Analysis for synchronous/asynchronous clocking schemes
- d. Timing analysis for analog/mixed-signal design

Efficient and accurate timing analysis solutions for emerging circuit implementation styles, process technologies, and manufacturing variations are needed. Timing analysis accuracy in the presence of process and statistical variations should consider realistic models of variations, as well as logic correlations for implementing false path analysis, multiple input switching. Analysis is needed to address productivity and timely processing, accurate layout modeling and estimation, hybrid synchronous/asynchronous clocking schemes, and heterogeneous designs.

3. System-Level and Logic-Level Synthesis

- a. Better physical metrics to drive logic synthesis and technology mapping
- b. Synthesis for new CMOS techniques (3D, variable back bias, multiple voltages, etc.)
- c. System-level synthesis, planning and estimation, including multicore design techniques
- d. Physically aware microarchitecture description and synthesis
- e. Tools for asynchronous and partly synchronous paradigms
- f. Memory design and analysis tools

Better system-level design tools are key to increasing designer productivity. Synthesis is needed which comprehends power, variability, gate and wire sizing, repeater insertion and placement, signal routing, global and local interconnect structures, signal integrity, and cell place and route simultaneously. Algorithms need to understand and optimize for power and be

cognizant of the impact of high-level design decisions on overall interconnect. Variable accuracy, on-the-fly RLC extraction and analysis are needed to incorporate the impact of the wire design on noise and timing.

4. Power and Clock Distribution Design Tools

- a. Techniques for power distribution in the presence of inductance
- b. Power grid design tools for selective power reduction
- c. Tools to support innovative clock design for 20GHz and beyond
- d. Tools to support alternatives to conventional synchronous clocking, multiple clock domains with different characteristics, etc.
- e. RF clock distribution techniques dealing with different phases

Power grid solutions are needed that provide for the unique power delivery and dissipation requirements across the chip while ensuring reliability concerns are addressed, optimizing for noise, power delivery at the module level, integration with place and route, taking into account inductance, variability, and reliability. Similarly, clocking methods are needed which reduce power consumption, address reliability through hybrid (asynchronous/synchronous) schemes, synthesize clock trees meeting prescribed skew, and process and manufacturing variations.

5. Tools for Robust Design for Manufacturability

- a. Yield-aware and yield optimization tools
- b. Design closure comprehending the effects of manufacturing variability, including synthesis and place and route mitigating the impact of random, systematic and environmental variations.
- c. Design techniques optimizing performance over a full range of process, voltage, and temperature
- d. Resolution enhancement techniques and related effects
- e. Defect-tolerant tools, resistant to static and dynamic faults (probabilistic design, single-event upset awareness, etc.)
- f. Noise, interference effects (inductance, skin effect, high frequencies, signal integrity, coupling)
- g. Tools for nanowires and nanostructures

Tools, even at the high level, need to be increasingly aware of the effects their decisions have on manufacturing. Research is needed on tools aware of yield effects, resolution enhancement techniques, tools comprehending inductive effects and other issues increasingly present as dimensions shrink. Tools are also needed to form or repair working circuits out of statically or dynamically defective sub-parts.

6. Fundamental Physical Design Techniques

- a. Physical design tools enabling predictable, correct-by-construction design flow from RTL to layout
- b. Place and route for mixed technologies
- c. Fundamental and significant place/route improvements
- d. Place/route for million-block designs

Solutions are needed to the traditional circuit design, synthesis and layout problems that enable robust, uniform, and predictable “correct-by-construction” design that requires little

analysis/verification overhead and few iterations, trading off some optimality for design techniques that result in predictable, guaranteed correct designs. Algorithmic innovations are needed for placement of millions of blocks in a reasonable time. As feature size get aggressively miniaturized, resolution enhancement techniques must be considered in place and route. In order to converge to a design solution while meeting performance demands, timing, reliability, signal integrity, and power as well as the clock tree design must be comprehended by the placement and route engine

7. Mixed-Signal, Analog, and RF Tools

- a. Tools to advance mixed-signal design
- b. Tools for automation of design of passives (MEMS, inductors, capacitors)
- c. Mixed-signal/analog synthesis tools
- d. Partitioning for mixed-signal design

Bringing automation tools (synthesis, layout, floorplanning, timing, etc.) up to the level of tools for the design of digital circuits and systems will be important to analog designers and to the design of heterogeneous, mixed-signal chips.

8. SoC and SiP Design Tools

- a. Consistent, intertwined tools for designing SoCs and SiPs
- b. Tools for SoC/SiP tradeoff analysis incorporating power, yield, thermal, timing, other considerations

New research needs to be developed to address the specific needs of SoCs and SiPs in the physical design arena, as there are few tools, flows and techniques that are specialized to aid the design of complex systems. The research needs include floorplanning and integration algorithms for SoC and SiP designs, timing analysis supporting mixed types of circuits, and algorithms and techniques to support IP reuse.

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