Research Challenges in Test and Testability
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Introduction

Test and design for testability are recognized today as critical to a successful design and manufacturing startup cycle, and it is understood that unless test is considered as an integral part of the design process, time to volume production will miss the market, the quality of the design will fail in performance or reliability, and the cost as a function of yield will exceed what the customer is willing to pay. Only by involving test planning and test development in all phases of design and manufacturing startup can a design be successful

University research is solicited to address the challenges which follow, and to address what members see as the three key areas on which advanced test work should focus:

1) Increasing test quality
2) Reducing test cost
3) Improving turnaround time and productivity

In the sections that follow, we outline the major research challenges in all fields of test. These challenges have been articulated by test experts in SRC member companies and have been organized to direct interested parties to appropriate topics. While this is not an exhaustive list, it represents the priority needs of the SRC community. Researchers are encouraged to utilize industry standard tools as a basis or reference point, and to specify clearly not only how their research goes beyond the industry state of the art, but also how they would put their results into practice in an industrial setting alongside existing methodologies and tools.

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1. Test in the presence of deep submicron effects and variability

1.1 At-speed test development for DSM

The industry widely uses two fault models (transition and path-delay) for targeting speed related defects or defects that affect the timing of devices. The fault models have their respective strengths and weaknesses, but it is imperative that the above two fault models be extended to capture some of the new defect mechanisms observed in DSM designs. Research in this area should address:

- small-delay defects below 90nm (faults to be targeted, patterns to detect such faults, and measures to indicate the quality of the test vector suite),
- new or updated fault models targeting different defective behavior due to new materials and transistor structures
- migration to smaller technology nodes (new methods to help determine whether structural tests can determine required margins when migrating, test sets to analyze the effect of design and process marginalities on manufactured parts, and identification of the cause of failures.)
- diagnosis of speed-related defects to identify paths that are actually failing in silicon due to at-speed defects to close the feedback loop so design or process changes can be made to improve yield.

Small delay defects represent a significant reliability concern when resistive defects are present in a technology. A low level of resistive defects can be overcome with typical TDF testing, however when the defect rate increases, traditional TDF testing is insufficient to achieve low DPPM levels. Today, additional stresses are necessary to age these defects to the point where TDF tests can screen them. In order to achieve low DPPM levels without additional acceleration such as burn-in, fine delay defect screening appears to offer a solution. Research is needed to create effective delay test patterns that are hazard-free yet maintain high coverage with significant increases to the pattern count. In order to effectively screen defects on very short paths, non-standard DFT techniques may be needed to create the necessary clock pulses.

1.2 Process variation

With DSM scaling, extreme process variation is predicted. Each device may have its own threshold voltage, and even devices physically together with the same orientation will have different behavior. Research is needed to explore the use of speed-related test methods to analyze the impact of process variation on actual silicon. The goal is to understand the source of variation and how to incorporate this knowledge back into the design flow (such as using path delay test measurements to calibrate timing analysis tools or to tune the DFM design rules) and how to optimize the selection of the test measurements while increasing the learning. How will test be carried out with a vast sea of unpredictable devices?

1.3 Statistical defect screening techniques

Techniques that process parametric test results for outliers have proven to be a very effective means of identifying defective material and providing a means for high quality and reliability without the need for burn-in. Current and future technologies will continue to reduce the effectiveness of existing techniques due to higher leakage and a reduced gap between the operating voltage and the threshold voltage. The biggest opportunity for improvement is not in the processing of the parametric data but rather in test patterns, environmental conditions and the measurement techniques that will be used to generate the data. Fundamental research is needed to understand what changes are necessary to current test practices to continue to make these techniques viable or find ways to augment or replace them.

Modern process technologies invariably lead to process variations that confound our ability to make a meaningful pass/fail decision at the time the manufacturing tests are being applied. The industry must move from simple go/no-go testing to treating wafer probe and final test as extended forms of metrology that are merely a data source to downstream die dispositioning that is more sophisticated and statistical in nature.

1.4 Systematic defect modeling and test

Defects in future DSM silicon scaling are trending toward more systematic (versus random) for reasons not fully understood. It is suspected that this trend is not due to the fabrication processes but could be the result of advanced lithography and new devices, or other DSM effects. In any case systematic defects affect a large number of die and research would be valuable into understanding and addressing these defects.

1.5 New ATPG techniques

Traditionally, structural patterns are used to test DSPs and complex SoCs, but functional patterns may also be used to test and debug hard-to-detect defects. For instance, if crosstalk effects are not considered, a chip may pass structural and functional patterns, but a field failure may still occur. In addition to testing the critical paths, techniques must also model other functional use conditions in the rest of the design to effectively catch such hard-to-detect defects. Generating such efficient functional patterns is be a challenging task and can be significantly expensive. New automatic test pattern generation techniques are required to maximize such effects while still guaranteeing high fault coverage and low pattern count. In addition to defect screening, these new patterns must also assist in diagnosis and failure analysis.

As designs are getting larger but time-to-market is getting shorter, more performance and memory optimization from test generation and fault simulation are needed. Research areas are optimizing TG/FS for multi-core microprocessors to use more parallelization, and use of SAT algorithms in conjunction with ATPG for test generation, especially to address hard-to-detect faults, timing constraints during test generation, and text compression.

The industry has attacked speed paths with AC ATPG patterns, LBIST, and FBIST, yet in many cases slow and costly system-level test is required to find the last 5% of functional faults. Is there a design methodology or tools that would allow any structural testing to reach 100% coverage?

2. Coverage and test methodology

2.1 Stuck-at pattern effectiveness

Examine and categorize fault types in 45/32nm and what the industry test can expect if coverage is restricted to DC patterns, perhaps differentiating between bulk silicon and SOI.

2.2 Simple, pre-tape-out IC quality model that permits test planning and trade-off analysis

Design and test engineers have at their disposal an array of test types and test methods for all components of an SoC – logic, memory, and analog circuitry being the simplest way to classify the die functionality. Depending on the product type and application, the customer-acceptable quality level in terms of time zero test escapes can vary greatly from near zero to hundreds or even thousands of defective parts per million (DPPM). Techniques are needed to decide which

DFT features and test types to use, and in what combination, in order to achieve the overall quality level for a design. Examples: ability to predict RAM DPPM given simple design/test metrics such as the layout, bit cell count, and BIST alternatives that might be applied, selection of the various logic test approaches and coverages, such as stuck-at, bridging, N-detect, launch-from-shift transition test, launch-from-capture transition test, etc.

2.3 Known good die and reliability

Continued research into the ability to produce Known Good Die, studying what characteristics contribute to success with Known Good Die (low power, design with *x*% margin, trade off *x* performance for *y* yield, throw away *x* parts from uncertainty, etc.)

2.4 Memory test, especially at below 90nm

As geometries shrink, industry experiences more problems with memory, and more test escapes from BIST engines that implement only standard march. What algorithms or test techniques would be most likely to find the new fault types from deep submicron lithography and processing?

2.5 Test structure / scan chain verification

Chip designs still get to manufacturing test and the basic test structures on the chip fail. There is a need for a verifiable methodology for the user to follow to ensure the test structures will work, so a re-spin just for test is not needed. Some of the issues are: scan paths with timing violations, incorrect physical design with unconnected scan chains, and power issues causing scan tests to brown-out or experience IR drop.

3. Analog, mixed-signal, and RF test

3.1 Fault model-based test for high speed analog and RF

Research in this area should focus on lowering the cost of build of analog and RF circuits by evaluating the fail mechanisms, developing a correlation model between failure mechanisms and fab-related variance in process, fault models based on the failure mechanism, a test methodology to detect these faults at low cost, and a yield prediction tool for analog and RF circuits similar to the defect density-based yield prediction for digital circuits.

3.2 RF loopback for half-duplex systems

In systems where the transmit and receive functions operate at different frequencies, how can we perform Tx-to-Rx loopback testing (either through internal or external loopback structures) when the frequencies and power levels of the Tx and Rx ports are different? How can we address frequency translation/splitting, both transmit and receive at a centered frequency, and power level compatibility?

3.3 Alternative test methods for RF circuits

Traditionally functional test methods have been performed for RF circuits. We believe there are opportunities for "alternative methods" which includes measuring non-functional parameters to predict functional parameters. These methods should be more cost effective and extendable to faster speeds.

3.4 Fast tuning

Frequency tuning via capacitor banks, DC and AC offset correction, often incur heavy test time

penalties in the production test process. How can these operations be performed faster?

3.5 BIST techniques for analog/mixed signal

For BIST of analog/mixed-signal components to provide substantial economic impact in reducing the cost of test, architectures must be explored in which self-test modes can be implemented in real commercial products without adversely impacting product performance or increasing product cost. Components must be implemented which occupy small area, have minimal current draw, and which do not have significant capacitance loading.

3.6 Efficient bit-error rate testing

Research is needed to explore techniques for efficient testing of digital transmitters and/or receivers at low bit-error rates in order to guarantee low BER.

4. System-level and SoC test and bring-up

4.1 System-level test and post-silicon validation

The complexity and heterogeneity of components within a system makes it mandatory to develop good test techniques to catch possible failures before it is shipped. Individual components may perfectly pass manufacturing test. However, when they are put together, testing these components along with their interfaces is absolutely critical. Structural test methods used for system test rely primarily on BIST. The industry needs a logic BIST solution that would guarantee good test quality at the system level. The solution should focus on reducing or eliminating the pain associated with the shortcomings of logic BIST (including problems of test point insertion, elimination of Xs, and failure diagnosis) and make it friendlier to design and test engineers. This would ease adoption of such a technology and help the industry maintain and predict the reliability of complex devices and systems both post manufacturing and at field.

Testing and debugging and diagnosis at the component and system level, including developing and inserting test hardware on the chip and on the board to increase the observability and controllability during system bring-up; inserting monitors, trace buffers, etc., with mechanisms for extracting debug data from the chip while the system is running, test generation and bug-isolation for systems with this additional hardware, and developing hardware structures that provide the ability to bypass errors inside the chip to continue testing for other bugs even after one bug is detected.

4.2 In-system test techniques for critical applications

In designs such as automotive products for mission critical applications and high end ASICs, customers mandate the requirement of having capabilities to run structural tests in the system, in a lab environment or in the field. Traditionally, this has been implemented with as separate logic BIST and memory BIST for memory portion. Disadvantages with this approach are X-intolerance, extreme difficulties with timing closure, and significant amounts of logic introduced on functional critical paths. There is a need to build intelligent on-chip compression schemes that are feasible for use in a system test environment, and if developed, can be adopted on a wide range of applications.

4.3 System level functional test coverage metric and grading

The goal of system test is to either screen defects which are not caught through regular, structural testing or to validate the design on a platform. Such tests are compiled using gross metrics (tests to cover a new feature) or incrementally generated based on customer fallout. Detailed coverage metrics are necessary to proactively determine when there is enough system content, and if deficiencies in coverage are highlighted ("test holes"), to guide generation of additional content. Currently no such coverage metrics exist and content is either reactively added or removed based on empirical evidence. Tangible progress in this area will require significant innovation since straightforward re-application of existing fault models and simulation methods will be inadequate. For instance, system test content consists of trillions of cycles hence detailed logic simulation is not feasible. Additionally, low-level fault models such as stuck-at and transition may be irrelevant or too burdensome for fault simulation of system test content. What is needed is fresh thinking in terms of high-level (architectural and micro-architectural) fault models and simulation methods, and possibly the use of workload sampling or tracing techniques for simulation of smaller, representative samples of the content.

4.4 Economics of BIST techniques for SoC

Today, BIST implemented discretely for logic, memory, analog, mixed-signal components, is not re-usable, leading to significant area impact for heterogeneous SoC designs. A reconfigurable BIST engine to test a variety of components is an attractive solution to SoC testing.

5. Test for process learning

5.1 Test for yield learning and improvement

As the feature sizes are reduced, systematic mechanism-limited as well as parametric issues begin to appear as substantial components in yield loss. Research is needed to explore:

- high quality test generation by linking the layout information with the ATPG process such that areas of the design prone to defects are exercised by the patterns, and defects are distinguishable to provide easy localization.
- statistical analysis techniques based on the production test failures and their diagnosis to determine the relative priority of yield limiting issues and the failure rates of various yield limiting features.

There are also good opportunities for test to enable faster learning using methods beyond what have been used historically. Faster learning may include yield, reliability, quality/DPM, defects, process variation and design margins. The priority of learning rate is much higher today for many products (particularly early in technology development). Most diagnostic methods today are based on "collect fail data from existing test patterns that were originally created to optimize test time/quality". Some of these methods should exploit "adaptive data collection." Clearly if we redefine the role of testing to include maximizing learning rate, there are many research and development opportunities related to testing.

5.2 Diagnosis for test learning

In recent years test has transitioned to have more of a metrology role: the manner in which a die fails may be recorded and analysis is done for both memory fail data and scan fail data, with decisions regarding yield limiters made based on the behavior. A fault model may then be described and can be analyzed and associated with a particular physical defect. Industry is at present lacking the information required to make the translation between failing data and failing

behavior. Proposals should focus on how to effectively turn failing data into failing behavior. Some of the requirements will be:

- Maximizing the ROI on collecting failing data, generating diagnosis targeted pattern sets, optimizing the number of failing cycles collected, etc.
- Correlating failing data with failing behavior for a single failing data log.
- Techniques for tracking behavior over time or correlating the behavior with changes in processing.

6. Test and power

6.1 Power dissipation during test

Power during test is a major concern since in the test mode the entire circuit is active and switching at the same time. This is not an issue during functional mode of operation as circuit operation is controlled and different parts of the circuit are shut-off to prevent both average and peak power dissipation beyond a pre-determined level. Studies show that during test, the power consumption can increase between 3-5X of the functional mode of operation. Power dissipation and its effects during test include clock tree power dissipation, power dissipation during scan shift mode, and power dissipation during scan capture mode. Power issues during test manifest themselves in various forms, including di/dt problems, voltage drop, and increased temperature. Research in this area should concentrate on developing methods and techniques to perform test without impacting the power profile of the device. Emphasis should be given on at-speed test application as it creates more of a power bottleneck.

Power dissipation may be much higher than normal in test mode if multiple blocks are targeted simultaneously to decrease test time. Increased power dissipation may cause an increase in temperature, voltage drop, and crosstalk, among other effects, far beyond the requirements necessary under normal chip operation causing failure during test. Power and noise management during test are critical for successful application of BIST, scan-based at-speed tests and SoC tests. Design, test scheduling and test vector generation techniques to manage power and noise during test must be devised.

The memory BIST patterns used to test memories today have been in use for many years. Most of these test strategies were developed to maximize fault coverage and reduce test time. Being efficient at testing, they also tend to consume a lot of power. A compounding factor is the fact that embedded memories are much bigger today than years ago. What improvements could be made in MBIST patterns/testing strategies to account for power consumption issues?

6.2 Test and power management

With exploding power numbers for processors and ASICs following not far behind, there are good research opportunities related to power management and power assessment at test. Note that testing may be the worst case condition because of the requirement for high-voltage stressing, increased circuit activity at test due to scan design and challenges related to thermal control at wafer and package test. In addition, an important requirement is to accurately assess device power (i.e., to accurately understand the device's power in functional operation). Research opportunities include:

- DFT for power management methods and tools for understanding power density

- cross-chip power variation and temperature variation during testing
- methods for stressing and detecting defects given power boundaries

Many chips incorporate various power-saving features such as multi-Vdd, multi-frequency, sleep modes, state retention registers, etc. How do we effectively test those chips in all these modes of operation without substantially increasing test cost? How can we test the many steps of power control in a timely manner?

7. Test for new applications and new technologies

7.1 Testing and DFT for 3D packaging

3D (silicon layering with through silicon vias) appears to be a leading contender to higher level of silicon integration that requires high performance (bandwidth and data rate) circuitries. This can potentially replace conventional scaling should there be a roadblock to technology scaling, so there may be a wider application potential. The current assumption of not testing the individual wafer (before wafer bonding) will become a yield limiter, especially if more than two layers of silicon are involved. Testing of partial circuits without a complete clock and power hookup is a big challenge. This is an expansion of the Known Good Die problem.

7.2 Testing for non-deterministic device behavior

Highly power managed devices are increasingly common among both power conscious as well as high performance systems. These devices will control the internal clocks accordingly to the internal power dissipation or other environmental factors (e.g. effectiveness of cooling). More and more chip interfaces are also changing over from parallel (e.g. buses) to packetized, serial signal engineered links (PCI Express, SATA, etc.), which may run at different clock frequencies than the core logic. All these can introduce nondeterministic device (functional) behavior, which is detrimental to conventional stored response testing. Structural testing solutions cannot cover these device features either.

7.3 Testing for aggressive / adaptive designs

This research would be focused on designs that are pushing the margins of performance and power and which may be most affected by impacts of variability. These designs won't have simple, fixed specifications differentiating good/bad devices. For example, as methods like statistical timing are used it may be important to understand the performance distribution and how variation can change critical paths. Additional data may have to be collected at test, which will also lead to research into how to perform adequate testing without slow parametric data collection. In addition, these chips will have "adaptive design" circuitry to enable adjustments to speed, power and margin (e.g., on-chip voltage regulation, temperature compensation, speed adjustments, clock gating). Today, it is not well-understood how to test devices which have these adaptive design features.

7.4 Test and security

Security challenges are escalating with the proliferation of mobile devices and are expanding beyond government, financial, and health care applications to all other domains. Test, debug, and failure analysis have always been historically at odds against information assurance: controlability and observability are properties desired for test, debug, and failure analysis, but are

extremely dangerous for information assurance. There have been cases of systems where critical security features have been bypassed or extracted by using scan chains and test modes. Though information assurance has been regarded as separate task for security engineers, there should be some research in the test area to address collaboration between security and hardware engineers in order to improve the overall robustness of the system.

7.5 Test in the presence of massive parallelism

The industry is moving to very high degrees of parallelism, at least during wafer probe, and not only for memory-only products but for logic and SoC products as well. These changes demand new methods for time zero and reliability die dispositioning with high selectivity/low overkill, new tester and database architectures which enable very high speed and accurate data collection and archiving, and models which demonstrate the impact of radical changes in the test flow such as no-stop-on-fail in light of the massive parallelism that is now being undertaken.

7.6 Run-time validation, diagnosis and correction

Device degradation (e.g. NBTI) and infant mortality (due to ineffective burn-in) are some of the issues that cannot be resolved with a time zero manufacturing test. These prompt the need for On-line (run-time) or temporary off-line self test (since it is in the field, end application), diagnosis, and correction scheme. The requirements for this fault resilience are different than traditional fault tolerant since faults are not transient (rollback won't work), nor static (degradation results in a slower device).