# SRC Research Needs in Computer-Aided Design Tools

## November 2007

The Semiconductor Research Corporation's Global Research Collaboration is seeking innovative research leading to significant advances in **System-Level/High-Level Tools** and **Logic/Physical Design Tools**. Needs categories of interest to the members are listed in the two tables below.

In accord with the SRC strategic plan and member development of this needs document, the Computer-Aided Design and Test Sciences area is placing renewed emphasis on system-level and high-level design. To this end, as we conduct our usual solicitation for logic/physical design tools, we introduce the new system-level, high-level design category. This stresses tools to facilitate higher-level design, and may include system-level verification and test tools.

Areas that SRC GRC member companies anticipate sustained or increased efforts in the coming five-year period include resilient design (with awareness of variability and statistical effects and the manufacturing interface), analog/mixed-signal/RF design tools, and tools for SoC and SiP designs. There is also member interest in areas where research is needed to enhance design automation tools to address technology advances such as 3-D, FinFET, double gate, etc.

Several themes important to SRC GRC member companies pervade the categories and subcategories below:

- Tools taking advantage of **parallel/multi-core platforms**
- Power aware/**power reduction** tools at all levels
- Tools incorporating **robust optimization** techniques

## CADTS Research Needs: System-Level/High-Level Tools

| 2007 System-Level/High-Level Tools Needs Categories | |
|---|---|
| **H1** | **Tools for Design Space Exploration** |
| H1.1 | Early design space exploration tools, including evaluation and estimation of architectural paradigms, partitioning for mixed-signal, SoC and SiP (including 3-D) |
| H1.2 | Tools for hardware/software partitioning and support re-configurability and repair |
| H1.3 | Tools for system-level tradeoff analysis incorporating power, yield, thermal, timing, performance, etc. |
| **H2** | **Tools for System-Level Design** |
| H2.1 | Behavioral and system-level design and synthesis tools (pre-RTL), including incorporation of hard/soft IP blocks |
| H2.2 | Tools for the design of multi-core systems |
| H2.3 | High-level SoC/SiP design tools, including analog/RF/mixed-signal sub-systems |
| H2.4 | Design tools enabling system-level to/from lower-level communication and abstraction |
| **H3** | **Tools for System-Level Verification and Test** |
| H3.1 | Tools for system level validation/verification of correctness, performance and robustness |
| H3.2 | System-level design for test and post-silicon validation |
| **H4** | **Tools for System Design Robustness** |
| H4.1 | Design tools that implement reliable resilient systems with non-functional or unreliable components |
| H4.2 | Design tools for systems using components with significant variations |
| H4.3 | DFM/DFR tools at higher levels in the design flow |
| **H5** | **System Power Optimization Tools** |
| H5.1 | Efficient system-level power management tools |
| H5.2 | Tools for efficient system-level control of power and elimination of hot spots |
| H5.3 | Tools that optimize supply voltage, frequency and Vt domains at the system level |

## CADTS Research Needs: Logic/Physical Design Tools

| 2007 Logic/Physical Design Tools Needs Categories | |
|---|---|
| **L1** | **Core/IP Design Tools** |
| L1.1 | Advanced logic synthesis, including for 3D, variable back bias, multiple voltages, etc. |
| L1.2 | Fundamental/significant place/route improvements |
| L1.3 | Tools for clock/power distribution/optimization, including those enabling alternatives to conventional synchronous clocking schemes |
| L1.4 | Tools addressing power/thermal considerations |
| L1.5 | Memory design and analysis tools |
| **L2** | **Analog/Mixed Signal Design Tools** |
| L2.1 | Analog synthesis |
| L2.2 | Tools for automation of design of passives (MEMS, inductors, capacitors) |
| L2.3 | Advanced analog simulation |
| L2.4 | Multiple voltage analog design tools |
| **L3** | **Design/Manufacturing Interface Tools** |
| L3.1 | Yield-aware and yield optimization tools including resolution enhancement techniques |
| L3.2 | Design tools exploiting lithography/mask knowledge |
| L3.3 | Tools mitigating noise, interference effects (inductance, skin effect, high frequencies, signal integrity, coupling) |
| L3.4 | Design closure tools comprehending the effects of manufacturing variability |
| L3.5 | Tools enabling defect-tolerant designs resistant to static and dynamic faults (probabilistic design, single-event upset awareness, etc.) |
| **L4** | **Tools for Diverse Technologies and Applications** |
| L4.1 | Tools for design using innovative CMOS nanostructures |
| L4.2 | Logic/physical/circuit design tools for diverse applications |