# Logic, Physical, and System Design Tools

**SRC GRC CADTS Needs**
**May 2011**

The Computer-Aided Design and Test Sciences area of the Semiconductor Research Corporation's Global Research Consortium is seeking innovative research leading to significant advances in logic, physical, and system design tools to benefit its member companies. Fundamental advances in tools, techniques and models that reduce cost and time to market, that lead to productivity improvements, and that enable designs higher in "quality" – better performance, lower power, more reliable, etc. – are welcome.

White papers are being sought advancing tools:

- In high-level/system-level design to improve productivity and reduce cost for stand-alone and embedded applications
- At the interface between design and manufacturing, overcoming the challenges of increasing system size and complexity
- Exploiting technology advances: 3D insertion, advanced CMOS nodes (14nm and beyond), and post-CMOS approaches

Note that different member products and segments may be produced at different technology nodes, so tools that support getting more performance and reliability out of existing technologies are also needed.

SRC is seeking proposals in common circuit-level tools (spanning both analog and digital designs), digital and analog design tools, and system-level tools. We have listed challenges in each of these areas that are barriers industry needs to address. These areas are not necessarily disjoint, and proposals may address challenges in multiple areas. These lists also do not imply that funding will be equally distributed among them, or that they are in any priority order; there are more topics listed than we will be able to support with projects. The goal is to attract forward-thinking proposals that address these member needs into the future.

Please note that embedded in these needs may be objectives that pull in different directions. For example, tools need to comprehend detailed electrical and other characteristics that may have been previously ignored, while at the same time tools for improving productivity often need to hide these details from the designer.

Verification and test are addressed in separate solicitations.

## Common Tools

C1) Electrically aware design rules and models, including extraction and modeling of manufacturability requirements specific to design needs, design rules for specific design / performance targets, etc.

C2) "More than Moore" tools for integrating heterogeneous designs on the substrate including digital, analog, RF, MEMS, etc.

C3) CAD tools using parallel algorithms, including multicore CPU/GPU

C4) Tools, methodologies and models that address power dissipation/leakage /thermal at all levels, including 3D

C5) Tools for signal integrity analysis and noise mitigation for multiple sources of interference (inductance and other high frequency effects, skin effect, coupling, etc.)

C6) Tools and models for addressing quality and reliability issues, including electro-migration, aging effects, etc.

C7) Design and design closure tools that address manufacturability/variability at all levels, including 3D and TSVs.

C8) Yield-aware and yield optimization tools including resolution enhancement techniques

C9) Design tools exploiting lithography/mask knowledge, including faster OPC and lithography algorithms

C10) CAD and optimization techniques, models and approaches for *novel* lithography, semiconductor manufacturing steps, and devices, memories, and interconnects

## Digital Design Tools

D1) Advanced logic/physical synthesis and cross-boundary optimization, including 3D, multiple voltages, etc.

D2) Automated synthesis and layout for datapath (custom-like) designs

D3) Support for multiple operating modes and power management techniques

D4) Memory design and analysis tools, including design and analysis of resilient architectures, error correction methods etc.

D5) Fundamental/significant place/route improvements, including how to scale the methods for multi-core designs

D6) Physical extraction and timing models for package, SiP, 3D

D7) Design closure tools for multi-core designs

D8) Tools and algorithms that address circuit marginality resulting from scaling and environmental effects

D9) Tools that take OPC and DFM into account earlier in the design flow, in logic and physical design

## Analog Tools

A1) Tools for modeling and automation of design of multiple passives (MEMS, inductors, capacitors)

A2) Advanced simulation tools for analog design

A3) Analog synthesis (integrated with verification) and optimization, taking into account designer intent

A4) Adaptive optimization methods determining on-the-fly what optimization methods to use based on the topology and design needs, including “designer-in-the-loop” optimization tools.

A5) Tools for the evaluation and design of 3D SoCs containing AMS and digital

A6) RF and millimeter wave design support for 2D and 3D chips

A7) Thermal behavior analysis for passive devices

A8) Tools addressing noise in mixed-signal designs

A9) Tools for analog DFM that focus on critical devices (matched pairs, current mirrors, etc.) and minimize unaccounted exposure to random and systematic variations (e.g., layout dependent effects).

## System Tools

S1) Planning, exploration, and design tools for homogeneous/heterogeneous 3D and multi-core systems, including innovative and efficient communication fabrics, clock distribution, etc.

S2) Tools for system-level tradeoff analysis and design, incorporating power, yield, thermal, timing, performance, etc., including software, real-time and embedded systems, heterogeneous SoC, SiP, 3D, and silicon-package co-design

S3) Tools for hardware/software partitioning, and processor/accelerator partitioning, supporting re-configurability and repair

S4) Tools and methodologies for design of systems that trade correctness for power and yield

S5) CAD for cyber-physical systems

S6) System-level tools addressing reliability and resistance to failure, including software reliability

S7) System-level tools addressing thermal and power analysis and reduction and electromigration.

S8) Tools that optimize supply voltage, frequency and Vt domains at the system level along with manufacturability, reliability, and power considerations.

## Contributors

| | |
|---|---|
| AMD: | Yaping Zhan, David Newmark |
| Freescale: | Savithri Sundareswaran, Puneet Sharma |
| GLOBALFOUNDRIES: | Rasit Topaloglu, Nicholas Eib |
| IBM: | Gi-Joon Nam, Haifeng Qian, Sani Nassif |
| Intel: | Jeff Parkhurst |
| Mentor Graphics: | Roberto Suaya |
| Texas Instruments: | Srinivasa Sridhara, Lawrence Arledge, Snehamay Sinha |
| SRC: | William Joyner, David Yeh |