Research Challenges in Test and Testability
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Introduction

Test and design for testability are recognized today as critical to a successful design and manufacturing startup cycle, and it is understood that unless test is considered as an integral part of the design process, time to volume production will miss the market, the quality of the design will fail in performance or reliability, and the cost as a function of yield will exceed what the customer is willing to pay. Only by involving test planning and test development in all phases of design and manufacturing startup can a design be successful.

University research is solicited to address the challenges which follow. These challenges have been articulated by test experts in SRC member companies and have been organized to direct interested parties to appropriate topics. While this is not an exhaustive list, it represents the priority needs of the SRC community. Researchers are encouraged to utilize industry standard tools as a basis or reference point, and to specify clearly not only how their research goes beyond the industry state of the art, but also how they would put their results into practice in an industrial setting alongside existing methodologies and tools.

In the outline, • indicates a very important topic to a member, and **o** indicates an important topic.

Acknowledgements

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1. Test and Manufacturing Process

1.1 Test and diagnosis for yield learning and improvement

The number of chip suppliers collecting and analyzing test data for the purposes of understanding and improving yield continues to grow. This is the result of the three trends in the industry. First, new generations of process nodes have proven to be more challenging to ramp yield than previously expected. Second, the continued increase of cost and cycle time associated with physical failure analysis (PFA) of ever smaller geometries necessitates better failing device selection and more knowledge about the failure mechanism prior to performing PFA. Lastly, commercial tools which provide economical and automated collection and analysis of test data have steadily become available in the last few years. Because of these trends, the need and opportunity for research in this area is also growing. There are three main research opportunities in this space.

1. *Cost effective data collection in the presence of embedded test* - While the desire is to have zero test cost (time) data collection, in practice, a limited test cost is tolerated but acts to limit the amount of data being collected in a production environment. There is a need to increase the amount of value obtained for a given test cost. At the same time, embedded test mechanisms such as compression and BIST introduce new challenges in collecting large volumes of valuable test data with little or no production test cost impact. Methods should be investigated that maximize the value vs. cost tradeoff and should specifically consider embedded test. Possible research directions to address this need include (but are not limited to) additional on-chip (Design-for-Test-Learning) or off-chip (ATE) hardware, developing production test patterns that balance the needs of production test and test learning, or improved manufacturing test procedures which dictate when and how much data to collect.

2. *Support for advanced failure mechanisms in diagnosis* – Advanced technology nodes have introduced many new failure mechanisms which do not behave in a manner consistent with the point defect mechanisms that most modern diagnosis tools primarily address. New diagnosis techniques should be investigated to deal with these new failure modes such as power droop, parametric shifts, and increased process variability. There are two main challenges to address. First, unlike point defects, these new failure mechanisms may cause a large number of simultaneous faults. A diagnosis procedure should be able to identify all the locations of all these simultaneous faults. Second, a diagnosis procedure should be able to attribute these failing locations to a specific mechanism. The identification of the failure mechanism is far more valuable for yield analysis than the location of the faults.

3. *Statistical analysis of a volume of diagnosis data* - During the process of diagnosis, it is typically not possible to identify the exact nature of the failure. A typical diagnosis result will reduce the number of possible failure mechanisms from hundreds to a few. However, recent research has shown that it is possible to get a correct understanding of the failure mechanisms in a population of devices through statistical analysis techniques. Much more research is needed in this area. Specifically, additional research is needed in how to combine diagnosis data with other data sources such as metrology, defect inspection, kerf structure, process equipment history, PFA results and other sources of process data.

Within the three areas of concentration identified above, research should be focused on emerging failure mechanisms. Some specific examples of the new breed of failure mechanisms include: process variation causing systematic defects, excessive power consumption, and performance yield tradeoffs.

1.2 Statistical defect screening techniques

Modern process technologies invariably lead to process variations that confound our ability to make a meaningful pass/fail decision at the time the manufacturing tests are being applied. The industry must move from simple go/no-go testing to treating wafer probe and final test as extended forms of metrology that are merely a data source to downstream die dispositioning that is more sophisticated and statistical in nature. Techniques that process parametric test results for outliers have proven to be a very effective means of identifying defective material and providing a means for high quality and reliability without the need for burn-in. Current and future technologies will continue to reduce the effectiveness of existing techniques due to higher leakage and a reduced gap between the operating voltage and the threshold voltage.

A number of aspects of this problem require further research. Some examples include, but are not limited to:
- Improved algorithms for outlier identification
- Faster methods for test data collection, both on die and off die
- Underlying test types and conditions used to generate the source data
- Comparisons of various alternatives using data derived from actual silicon
- Better information about screening methods and the types of defects they can and cannot detect

1.3 Systematic defect modeling and test

Defects in future DSM silicon scaling are trending toward more systematic (versus random). It is suspected that this trend may not be due to defects generated during the fabrication process in the traditional sense but instead may be the result of advanced lithography and other DSM effects. Process-design interaction resulting in differences in systematic defects on products with same/similar layout rules needs to be understood. This is important since achievement of high yield on a product does not guarantee similar yield of another product/derivative on the same process. In any case systematic defects affect a large number of die and research would be valuable into understanding and addressing these defects. The ability to rank design for manufacturability (DFM) checks to establish their relative importance in terms of the avoidance of time zero yield or longer term reliability losses in a given technology is of particular interest.

2. Coverage and Test Methodology

2.1 Pattern type effectiveness, optimization and selection

The number of test pattern types and methods has continued to increase over time but the acceptable amount of time and patterns used to test each die have not increased at the same rate, if at all. In particular, recent years have witnessed the introduction of several competing at-speed test methodologies such as faster-than-at-speed testing, tests generated using shortest path information, K Longest paths, and other small delay defect test methods which compete with traditional transition fault and path delay testing methods for test time. Furthermore, there are multiple clocking strategies which can be employed including tester-based, PLL-based, launch-from-shift, and launch-from-capture. Bridging fault tests are starting to see more attention and interest, and again there are many methods for generating the fault lists and tests and merging them with the existing test suite already used in production tests. And bridging tests are just one example of the more general class of defect-driven test methodologies. Research is necessary to develop methods for trading off test time and test type to optimize the test strategy for a device

given its performance, power, cost, and other product requirements, tester requirements and limitations, and defect paretos for the technology in which it is implemented. As in previous sections, it is very desirable to verify as much as possible the work results and outcomes on actual production silicon data and devices from a member company as opposed to mere fault simulation exercises.

2.2 Simple, pre-tape-out IC quality model that permits test planning and trade-off analysis

Design and test engineers have at their disposal an array of test types and test methods for all components of an SoC – logic, memory, analog circuitry, and perhaps high speed interfaces being the simplest way to classify the die functionality. Depending on the product type and application, the customer-acceptable quality level in terms of time zero test escapes can vary greatly from near zero to hundreds or even thousands of defective parts per million (DPPM). Techniques are needed to decide which DFT features and test types to use, and in what combination, in order to achieve the overall quality level for a design, and to be able to mathematically estimate the test escape rate with as much accuracy as possible. Logic DPPM models are fairly well understood when compared to memory, analog and high speed circuitry, so these latter types are of particular interest for further research.

2.3 Known good die and reliability

"Infant mortality" has been addressed in semiconductors through lengthy burn-in test insertions that stress the device through elevated temperatures and/or by voltage stress. From a Known Good Die (KGD) perspective, lengthy tests are generally prohibitive. As geometries continue to shrink there is a concern that voltage stress will lose its effectiveness. Research should address the ability to produce reliable KGD by studying either new acceleration techniques and/or quantifying the benefits of different design constraints (e.g. low power, design with x% margin, trade off x performance for y yield, throw away x parts from uncertainty, statistical techniques for reliability, and design rules to improve reliability.)

2.4 Adaptive test

New and aggressive design techniques and IC manufacturing technologies often result in increased variability of line widths, electrical parameters, product performance, and other important aspects. Some of the variations are permissible while others, while subtle and difficult to measure, are not. Traditional test methods with fixed limits, when applied in these situations, can sometimes either fail to identify these failures or can "overkill" by misclassifying as fails devices with tolerable variation. Research is necessary to continue to develop and refine methods which can allow the test process to be varied in much the same way as the products to which it is applied. One area of research, statistical methods, is already discussed in Section 1above. Besides these approaches, much work remains to be done. Flexible manufacturing flows which can adapt to constantly changing material and product requirements must be developed. Faster and less costly methods for collecting production test data that feeds these processes must be deployed. These solutions could be either on-die or off-die or both and would require supporting infrastructure components such as databases and rapid access methods for feed-forward and feedback among test steps. Automated monitors and decision strategies are needed to alert when control limits are exceeded and to govern insertion and/or removal of test content within a particular test insertion and also possibly between insertions.

2.5 At-speed test development and application

Over the last few years, the industry has started adopting at-speed tests specifically to target speed related defects that have become prevalent with smaller technology nodes. Stuck-at patterns are no longer sufficient to achieve high defect coverage since defects such as resistive bridges, resistive vias, power droops, cross-talk noise effect, etc., are manifesting in subtle timing changes that can only be detected using at-speed tests. Timing aware fault models have also been proposed to target small-delay defects that represent a significant reliability concern when resistive defects are present in a technology node. Although such fault models are available to address some of the speed related concerns, there are still numerous challenges that need to be solved before it can be widely adopted across the industry. Research in this area should focus on the following topics.

1. One of the challenges for at-speed test is to explore whether it can be used for speed binning, thereby reducing the dependency on functional tests. There has been some progress but it remains to be determined how one can generate and apply at-speed tests closely resembling the functional mode of operation.
2. Power related effects, switching activities, and temperature profiles along with other environmental factors affect the timing of a device for a given test set. At-speed tests should be applied under conditions that mimic the functional operation in order to reduce any yield loss associated with at-speed scan tests. Can we come up with a scan-based at-speed solution which will generate at-speed test patterns that are compliant to design constraints including those for timing, layout, and power?
3. Timing-aware fault models usually try to propagate the fault effect through the longest path based on the timing information. However for smaller technology nodes, because of process variations it is difficult to predict timing critical paths, as paths that are not critical based on design/ simulation may suddenly become critical and speed limiting. At-speed tests should not only be able to detect random defects resulting in timing anomalies but should also be able to isolate defects that are more systematic in nature and are a consequence of process variations.

2.6 New ATPG techniques

Traditionally, structural patterns are used to test complex SoCs, but functional patterns may also be used to test and debug hard-to-detect defects. For instance, if crosstalk effects are not considered, a chip may pass structural and functional patterns, but a field failure may still occur. In addition to testing the critical paths, techniques must also model other functional use conditions in the rest of the design to effectively catch such hard-to-detect defects. Generating efficient functional patterns is a challenging task and can be significantly expensive. Therefore, research in ATPG should focus on improving the quality of test patterns such that the dependence on functional patterns is greatly reduced.

1. New automatic test pattern generation techniques are required to target hard-to-detect failures while still guaranteeing high fault coverage and low pattern count. In addition to defect screening, these new patterns must also assist in diagnosis and failure analysis.
2. In the past, the introduction of new fault models directly translated into additional patterns that are a result of targeting such faults during ATPG. Consequently, the pattern count increases as newer fault models are expected to improve the overall defect coverage. Moving forward, ATPG techniques should be improved to develop compact pattern sets that would provide a robust coverage of not just a single fault model but a variety of fault models thereby improving the overall defect coverage.
3. As designs are getting larger but time-to-market is getting shorter, more performance and memory optimization from test generation and fault simulation are needed. Research areas

are optimizing TG/FS for multi-core microprocessors to use more parallelization, and use of SAT algorithms in conjunction with ATPG for test generation, especially to address hard-to-detect faults, timing constraints during test generation, and test compression.

3. Analog, Mixed-Signal, and RF/High Speed Test

3.1 Metrics, models and methods for high speed I/O, analog and RF test

With increasing integration of diverse analog components on a single die including several PLLs, sensors, different high-speed communication interfaces, baseband, and RF, the proportion of area occupied by analog circuitry is significantly increasing and controllability is decreased. To ensure desirable outgoing product quality at an affordable cost, it is essential to test this circuitry adequately to address both defects and marginalities. There is a need for usable and automated metrics and methods to gauge the quality of test stimulus for testing these circuits in terms of their ability to identify and quantify deviation from normal functionality, or to systematically generate tests to target specific hardware vulnerabilities.   The need for new techniques for testing unidirectional interfaces are becoming more important given the increasing need for expensive test equipment in the absence of better methods. Metrics and models are needed at a level of abstraction that is adequate to capture a circuit's deviation from normal functionality, and at the same time not necessitating methods that are impractical due to reasons such as excessive simulation time.   Design-for-test methods are needed that enable controllability and observability of deeply embedded analog modules.   Due to falling product average selling prices, envisioned solutions should comprehend and minimize test cost. Techniques are needed that enable testing of analog front-end through digital interfaces thus lowering test cost through use of less expensive digital testers.

3.2 Innovative test for RF circuits including alternative methods, loopback

RF test can be still expensive compared to digital and mixed signal devices. To overcome this disadvantage there are few volume production-worthy test techniques published and accepted industry-wide. Alternative, alternate, loop-back techniques have been published along with some BIST and BIT techniques, but not implemented as a standard RF test technique. This topic is open to bring in new ideas on low cost test implementations. A theoretical and practical evaluation of the strengths and weaknesses of the proposed techniques will be required to demonstrate the advantage when comparing with established traditional RF test techniques. Parallel test techniques that reduce test time to test/measure front-end specifications are needed.

3.3 Fast tuning, calibration and repair

Analog circuits on silicon are characterized by their increased sensitivity to process drift. A large proportion of silicon failures are usually attributed to circuit parameter changes due to process drift rather than just gross defects. Analyzing circuit behavior during the pre-silicon design phase for different circuit parameter combinations over a wide range of process variations at a desired accuracy is usually expensive and impractical due to excessive simulation time. This necessitates the need for automated design-for-test-and-validation strategies to be used after first-silicon during bring-up (post-silicon validation) and during HVM (high volume manufacturing) test, that allow enough granularity of access to enable circuit parameters to be tuned in silicon to meet desired specifications, and not expensive in terms of power/performance or test cost.

3.4 BIST/BIT techniques for analog/mixed signal

Aspects to investigate include: (a) What instrumentation on tester can be incorporated on-chip as test infrastructure IP module? (b) How can such a module be re-used across different functions to be tested? (c) Can such modules be generated / created from programmable specifications for different test requirements? (d) How can software BIST be applied to analog / mixed signal circuits and what are the parameters / metrics for test and evaluation? (e) How comprehensively can BIST supplement conventional tests for test and calibration?

3.5 Adaptive test for analog/mixed signal

A typical test for analog/mixed signal devices is expensive compared to digital circuits and often the ATE is limiting the parallel test of multiple devices. One solution to bring the test cost in alignment with customer price expectations is to implement adaptive test flows. These adaptive test flows are defined as a test execution based on previous test results. These test results can be from other devices of the same manufacturing batch or the same device taken at the same test insertion or previous insertion tested at different temperature. This definition also included test flows, where the test stimulus will be adjusted to previous test results. The research on this topic should demonstrate new algorithms for decisions on test execution, yield prediction and an evaluation of DPPM.

3.6 Test for >50 GHz devices

New high data rate transceiver systems are in an early stage of development using open frequency bands of frequencies greater 50 GHz. Conventional test techniques where the ATE is supplying a stimulus and measures the response will be difficult to use at these frequencies, since the implantation cost will be tremendous. The research topics to overcome the difficulties of generating and transporting a stimulus accurately with frequencies greater than 50 GHz should be directed to low cost production test. Topics can include BIST techniques, on-die or on-wafer stimulus generation, on-die response analysis or wireless transmission for test. A practical demonstration of a prototype or demonstrator will be required to show the readiness of the proposed test technique.

4. System-Level and SoC Test and Post-Silicon Validation

4.1 System-level test, debug and correlation to tester

The complexity and heterogeneity of components within a system makes it mandatory to develop good test techniques to catch possible failures before it is shipped. Even though individual components may perfectly pass manufacturing test, when they are put together these components (along with their interfaces) must again be thoroughly tested. Structural test methods used for system test rely primarily on BIST. The industry needs improved system-level BIST solutions that guarantee good outgoing quality at the system level. In addition to logic BIST, other solutions include "functional-BIST" and broader use of embedded test structures at the system level. Improved BIST solutions should focus on reducing or eliminating the shortcomings of logic BIST (including problems of test point insertion, elimination of Xs, and failure diagnosis) and make its use friendlier to design and test engineers. This would ease adoption of such a technology and help the industry maintain and predict the reliability of complex devices and systems both post-manufacturing and in-field.

Currently functional test generation tends to be ad hoc and there is no systematic coverage metric to ensure test completeness and to ensure high quality test selection. Such a coverage metric, preferably computed using less computationally expensive high-level simulation methods is needed.

4.2 Post-silicon validation/bring-up

Post-silicon validation (or bring-up) of an integrated circuit is the process of validating silicon over several iterations with the goal of qualifying the product for manufacturing test. Each iteration of silicon is expensive in terms of delaying the time-to-market of a product. Validation for electrical marginalities is an important part of this bring-up process – the outcome of which has implications on testing including identification of high quality test content for test-volume and test-time limited manufacturing test. There is a need for system-level design-for-debug strategies and associated local controllability/observability hooks to enable not only automated root-cause of failures due to marginalities, but also automated methods to fix them on the same silicon if appropriate in order to progress beyond a bug to identify and fix others. Strategies that can identify and fix marginality issues can be envisioned at different appropriate levels of design abstraction (e.g., for a processor it can be at the hardware, microcode, assembly, or even the operating system levels). Strategies can involve inexpensive on-die data collection techniques and other failure-reporting hooks that pass information to bug-detection-and-servicing mechanisms.

4.3 In-system test techniques for critical applications

(a) While modular logic BIST and memory BIST are well investigated and well applied, there is a need to stitch together these modular solutions at the chip and system level. For example, how can the overall chip and overall system be completely tested in minimal time? (b) Is there a need for a system level test scheduler which can help stitch / create an optimal (compressed) test schedule for various components, for a given set of offline and online test requirements, depending upon which set of modules can be tested concurrently, and which of them cannot, and depending upon whether the tests must be run without being interrupted (start to end) or in interrupt mode (halt-resume)? (c) How adequately can such structural techniques be used to guarantee system correctness? Where / how should they be supplemented with system tests? (d) How is the quality of in-system test measured in terms of coverage, detection latency, robustness, etc.?

4.4 System level functional test coverage metrics and grading

The goal of system test is to either screen defects which are not caught through regular, structural testing or to validate the design on a platform. Such tests are compiled using gross metrics (tests to cover a new feature) or incrementally generated based on customer fallout. Detailed coverage metrics are necessary to proactively determine when there is enough system content, and if deficiencies in coverage are highlighted ("test holes"), to guide generation of additional content. Currently no such coverage metrics exist and content is either reactively added or removed based on empirical evidence. Tangible progress in this area will require significant innovation since straightforward re-application of existing fault models and simulation methods will be inadequate. For instance, system test content consists of trillions of cycles hence detailed logic simulation is not feasible. Additionally, low-level fault models such as stuck-at and transition may be irrelevant or too burdensome for fault simulation of system test content. What is needed is fresh thinking in terms of high-level (architectural and micro-architectural) fault models and simulation methods, and possibly the use of workload sampling or tracing techniques for simulation of smaller, representative samples of the content.

4.5 Economics of BIST techniques for SoC

Today, BIST implemented discretely for logic, memory, analog, mixed-signal components, is not used to eliminate significant test cost components. For example, an SOC may implement various BIST techniques, but still require scan, ATPG, functional testing, etc. Hence BIST is seen as an added cost. From an economic standpoint, one must look at the factors that contribute to the total cost of the product and assess if the addition of certain BIST features to the design will reduce the overall cost or improve quality. Proper assessment of these type of economic decisions may need to take into account the life cycle cost aspect of the SOC.

4.6 Design for functional debug, isolation and root cause

Structural testing remains an effective but sometimes incomplete method of weeding out bad devices. Functional tests may be required to detect device failures. There are also cases where failures only exist in a certain customer environment. The ability to quickly isolate the cause of either of these failures has great value. Preferably a functional failure would include enough diagnostic information that a shorter structural test could be constructed to reduce test time and/or improve test coverage in other similar areas. Opportunities might include on-die logic, physical access mechanisms, automated and more exhaustive attacks using structural tools or snippets of functional sequences.

5. Test and Power

5.1 Test and power management

With exploding power numbers for processors and ASICs following not far behind, there are good research opportunities related to power management and power assessment at test. Note that testing may be the worst case condition because of the requirement for high-voltage stressing, increased circuit activity at test due to scan design and challenges related to thermal control at wafer and package test. In addition, an important requirement is to accurately assess device power (i.e., to accurately understand the device's power in functional operation). Research opportunities include:
  - DFT for power management methods and tools for understanding power density
  - cross-chip power variation and temperature variation during testing methods for stressing and detecting defects given power boundaries

5.2 Test of low power devices and low power modes

Many chips incorporate various power-saving features such as multi-Vdd, multi-frequency, sleep modes, state retention registers, etc. How do we effectively test those chips in all these modes of operation without substantially increasing test cost? How can we test the many steps of power con trol in a timely manner? Perhaps we need Design for test features/standards to partition the problem and to enable testing low power features and modes in a systematic manner. How do we classify chips that pass all the tests but fail to meet their power goals? Is there a notion of "power binning" similar to frequency binning. Are there certain types of defects that attribute to these power-failing devices? Measuring power occurs over many clock cycles, so unlike timing, it is hard to pinpoint the specific part of the design that might be causing the problem. What is the appropriate level for doing debug/diagnosis to understand the cause of power-failing chips and to identify design/process trends that could be corrected?

5.3 Test for power delivery effects

Power delivery is increasingly a function of multiple factors, including VRM, motherboard, packaging and on-die parasitics, power gating, multi-cores, clock-gating and other power mechanisms. It is increasingly necessary to have test strategies that ensure that defects or marginalities in these multiple mechanisms, together or individually, do not cause a functional failure. Testing mechanisms may include creation of targeted functional/structural tests that stress power delivery vulnerabilities by exciting various scenarios (e.g., low and high frequency power droop, IR drop etc.), power delivery testing state synthesis, and power delivery failure diagnosis.

5.4 Test structures for on-die data collection, including thermal

The need for test-structure-based on-die data collection is driven primarily by (1) within-chip variation that limits the representativeness of scribe-line structures and (2) need to monitor chip behavior during operation and over lifetime. Complicated design-process interactions make product-based learning attractive, but test structures are also needed to provide additional data for both bring-up and yield-learning. Specifically, improvements are needed in structures that provide manufacturing process information, especially those that can distinguish the effects of different process parameters, those that provide run-time voltage and temperature information, and those that monitor reliability-related degradation.

6. Test for New Applications and New Technologies

6.1 Testing and DFT for 3D packaging

3D (silicon layering with TSV (through silicon vias)) appears to be a leading contender to higher level of silicon integration that requires high performance (bandwidth and data rate) circuitries. This can potentially replace conventional scaling should there be a roadblock to technology scaling, so there may be a wider application potential. TSV pads are not probe-able as a pristine surface is needed for subsequent bonding. Their size and pitch is also beyond today's mechanical probe technology. Hence, the strategy of not testing the individual wafer before wafer bonding is a significant yield limiter, especially if more than two layers of silicon are involved. Testing of partial circuits without a complete clock and power hookup is a big challenge. This is an expansion of the Known Good Die problem. Die level assembly is also a possibility for some devices, especially where multiple vendors are involved. It is highly desirable that test access be made only to the side that mounts onto the substrate though signals for normal operation may exist on both sides of a die. Due to lighter loading from die to die, I/O cells will be much simpler and smaller. Mixed technologies (digital, memory and analog) may be stacked.

6.2 Testing for non-deterministic device behavior

There are multiple reasons for non-deterministic device behavior becoming an issue at this point. 1) There is demand for increasingly complex and varied designs which has forced wider adoption of SOC practices. These complex chips may have high speed interfaces, wireless, video and audio components which desire different frequencies of operation. Any time clock domains are crossed there is an element of non-determinism. 2) High speed interfaces may have variable length training sequences that automatically adjust operating parameters to compensate for process variation and operating conditions and may include non-deterministic protocols. 3) Designs are increasingly sophisticated in their means to adjust their operating conditions to remain within a power or temperature envelope (see section 6.3 for additional examples). The cumulative result can put a

strain on traditional ATE in terms of generating conventional test vectors. It may also make it difficult to debug devices where techniques requiring fast deterministically repetitive signals are used. Forcing different IP blocks to run synchronously at degraded speeds to each other may create test coverage holes, particularly where performance testing is required. Research into protocol aware testers as well on-die DFT techniques are areas to investigate.

6.3 Testing for aggressive/adaptive designs

Power management circuitry is used not only for power minimization but in some applications for scaling power upwards to boost performance when the device application requires it. Circuit trimming for analog devices is another similar application of the notion of adaptive design. For the voltage scaling case, the amount permissible to raise supply voltage is not limitless but must be bounded several variables including timing closure frequencies and margins, reliability requirements, and other factors. Determining an aggressive but safe upper limit is a difficult problem. The default approach is to use a conservative upper bound but that may result in an uncompetitive product. There are many proposed methods for identifying and applying less conservative upper limits including time zero measurements of various types and on-die and in situ approaches that may be used periodically throughout the product's lifetime. The upper limit may not be a fixed quantity but might vary depending on the chip's aging response. At some point the product might need to determine and indicate that failure is imminent and that it should be replaced. More research is required to elaborate test methods and infrastructure to employ for lifetime performance management. And just as in the power management case, the infrastructure itself must be tested and correlated to the silicon performance it is intended to measure.

6.4. Test and security

Traditional testing of ICs is done using ATE (Automated Test Equipment). Those test methods are well characterized by a high flexibility, a small amount of additional hardware on-chip and proven high fault coverage for a certain test length.

Higher complexity of modern designs and the larger amount of test data makes it harder to perform high quality external tests. Moreover this approach is hampered by the difficulty in accessing internal design blocks. Also the needed higher application frequencies in actual and future designs results in more expensive test equipment.

But one of the major advantages of external test approaches is the excellent accessibility to all tested components for each kind of diagnosis through the test channels. Logic-Built-In-Self-Test (LBIST) can be used to overcome most of the mentioned disadvantages of external tests. The BIST technique is superior when applying on-line, in-field, or burn-in test

In addition LBIST is a primary choice for security applications like Smart Cards or crypto-chips. The main advantage here is the fact that each test can be applied without any external access point. Since such access possibilities almost always are not allowed for security applications.

The primary objective in this area is to investigate possibilities for an economic solution to efficiently combine the advantages of the proven LBIST technology and needed diagnosis approaches in such a way that future IC applications will be considered appropriately.

6.5 Test with parallel resources

The industry is moving to very high degrees of parallelism, at least during wafer probe, and not only for memory-only products but for logic and SoC products as well. These changes demand new methods for time zero and reliability die dispositioning with high selectivity/low overkill, new tester and database architectures which enable very high speed and accurate data collection and

archiving, and models which demonstrate the impact of radical changes in the test flow such as no-stop-on-fail in light of the massive parallelism that is now being undertaken.

6.6 Test for multicore chips

Single die with multiple instantiations of IP are increasingly common. The fundamental problem is the volume of test data. Some historical methods include pipelining and/or broadcasting inputs and collecting and/or comparing outputs. However these may not be the optimum solution to scale to large arrays of IP. Opportunities could include more capable on-die test management such as an IP core being capable of directing other tests. Solutions should comprehend not only test but also debug and data collection.

6.7 Validation, diagnosis and correction for both in-field and OEM survivability

While post-silicon validation (bring-up) and manufacturing test aim to ensure desired product quality, there are a few factors that can still cause failures either at the OEMs (system manufacturers) or at the end-customer. Reasons for failures at an OEM can be due to differences in the usage and electrical environment (such as the application content or the system platform) of a system at the OEM compared to the test environment of the component manufacturer. Currently, there is lack of good diagnostic methods to isolate failures to a particular component and, as a result, good components get shipped back to the IC manufacturer for debug. This results in an expensive and unnecessary debug process. Hence, there is a need for test and debug strategies that enable debug of a component (such as a processor) in a system environment without compromising intellectual property and security.   Permanent failures at the end-customer can occur prior to the end of the guaranteed life-time of a product due to device degradation (e.g. aging NBTI, electromigration) and infant mortality (due to ineffective burn-in). These are issues that cannot be resolved with a time zero manufacturing test. These necessitate in-the-field test and repair strategies - either concurrent (on-line) or off-line self test, diagnosis, and correction. Notable characteristics of such failures are that faults are not transient (rollback solutions are not appropriate) and manifest gradually (hence degradation can potentially be tracked). Strategies that address such failures need to comprehend their sensitivity to use conditions.

6.8 Memory test including standard SRAM and non-traditional technologies

Embedded memories continue to occupy significant real estate on a chip. The variety of SRAMs that are being used in designs are also expanding – especially with the advent of MRAMs (magneto resistive RAMs), FRAMs (ferro-electric RAMs), SGRAMs (synchronous graphic RAMs), VRAMs (video RAMs), nvSRAMs (combination of SRAM and EEPROM), PBRAMs (pipelined burst RAMs), etc. Research in the memory test area should primarily focus on the following areas.

1. There is substantial body of work showing different defect mechanisms that occur in SRAMs and the algorithms that can be applied to detect them. Further research is necessary to determine whether the existing algorithms can be used to detect the defect mechanisms that manifest in the newer RAM structures or newer algorithms need to be developed to target such defects.
2. Since the number of embedded RAMs in a design has increased substantially, testing of memories takes significant test time as well as silicon overhead. Current solutions consider one or more factors when determining an optimal test. However, the overall memory BIST architecture needs to consider test time, area overhead, power dissipation, routing overhead, programmability, repair, etc. in order to come up with an efficient test scheme. Research in this area should focus on optimizing the overall memory test architecture such that the efficiency with regards to test application time and the area overhead are greatly improved.

6.9 Testing and high voltage/current devices

Wafer processes are in development which will allow integration of circuits for the voltage range of up to 1kV. Some of these new devices will go into the commodity market where the test cost will be highly critical. It will be difficult to supply in a safe, cost efficient way these high voltages to a device under test (DUT). Research topics to overcome this difficulty might include BIST techniques but also DUT internal generation. A demonstration of the proposed technique would be beneficial to show the advantages and limitations.