Research Challenges in Test and Testability
Semiconductor Research Corporation
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Introduction

Test and design for testability are recognized today as critical to a successful design and manufacturing startup cycle, and it is understood that unless test is considered as an integral part of the design process, time to volume production will miss the market, the quality of the design will fail in performance or reliability, and the cost as a function of yield will exceed what the customer is willing to pay. Only by involving test planning and test development in all phases of design and manufacturing startup can a design be successful.

University research is solicited to address the challenges which follow. These challenges have been articulated by test experts in SRC member companies and have been organized to direct interested parties to appropriate topics. While this is not an exhaustive list, it represents the priority needs of the SRC community. Researchers are encouraged to utilize industry standard tools as a basis or reference point, and to specify clearly not only how their research goes beyond the industry state of the art, but also how they would put their results into practice in an industrial setting alongside existing methodologies and tools.

SRC seeks university research which is pre-competitive, and promotes interaction between faculty and industry to address challenges that members see in future systems and technologies.

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1. Test Cost and Quality Improvement

1.1 Novel design-for-test (DFT) methods

Despite the large body of research over the last 20+ years on Built-in Self-Test (BIST), there are still many barriers that prevent BIST from being a primary/sole testing method. These barriers include power, coverage, die area, timing convergence after physical design, poor awareness of the economics involved, etc. Researchers should explore novel methods to tackle those barriers. The scope of the solutions should encompass analog BIST, memory BIST, logic BIST (LBIST), in-field self-test and software-based BIST. Development of BIST solutions to (a) handle design timing exceptions such as multi-cycle and/or false paths, (b) address debug and isolation of speed issues and marginalities, and (c) shadow logic around arrays possibly through array-write-through, are needed. The long-term goal is to significantly lower test and post-silicon validation cost by reducing the dependency on expensive external test equipment, and by driving more and more test function onto the chips and systems.

1.2 Test cost reduction

Test costs will increase without new methods for cost reduction. Drivers of higher test cost include higher test coverage requirements, additional parametric measurements, and increased product personalization during testing. Aspects of test cost that should be targeted for cost reduction include:

- Generation: Time, memory, test data volume
- Grading: Fault simulation time and memory consumption
- Dfx: Area, design complexity, verification, yield degradation
- Application:
    - Test time
    - Test data volume (transfer time, test memory, pattern load/reload time)
    - Tester requirements (slow vs. at-speed, counters, current/voltage measurement resolution)
    - Data collection (time, volume)
    - Decision-making on tester (time, required computing power)
- Post-processing (Algorithmic complexity, dispositioning overhead)

1.3 Adaptive test

From ITRS Roadmap: Adaptive Test is a broad term used to describe methods that change test conditions, test flow, test content and test limits (potentially at the die/unit or subdie level) based on manufacturing data and statistical data analysis. This includes feed-forward data from inline and early test steps to later test steps and feedback of data from post-test statistical analysis that is used to optimize testing of future products. Adaptive Test also includes real-time data analysis that can perform Statistical Process Control (SPC) and adjust test limits and content during product testing on-the-fly. (e.g., Parts Average Testing algorithms) Although some simple applications have been applied for some time, Adaptive Test will increasingly be applied and will require updated software algorithms and complex statistical analysis methods and database infrastructure.

Adaptive testing is a rich area for research and has application addressing issues described in other sections including:

- Methods for test cost reduction (Section 1.2)
- Statistical screening methods (Section 1.4)
- Pattern type effectiveness and optimization (Section 1.7)
- Yield Learning / data collection (Section 2)
- Analog, mixed-signal and RF/high speed test (Section 3)
- Testing for resilient/adaptive systems (Section 7)

Research should target developing production-capable applications that optimize key metrics such as yield loss at test, reliability/DPM, test time/cost and test-driven data collection. Research is needed on design-for-adaptability (DFA) schemes that focus on design/test architectures and methods that facilitate flexibility during test application to dynamically adapt to test results.

1.4 Statistical defect screening techniques

Failures increasingly may not manifest as incorrect latch-captured values during test. Statistical defect screen techniques identify outlying die due either to defects or unacceptable process variation. Examples of needed research areas include, but are not limited to:

- Algorithms for outlier identification
- Test data collection methods, both on die and off die
- Underlying test types and conditions used to generate the source data
- Comparisons of various alternatives using actual silicon data
- Statistical methods that enable reliability-type failures to be detected without relying on burn-in
- Better understanding of screening methods and the types of defects they can and cannot detect

1.5 Known Good Die and reliability

Known Good Die (KGD) refers to the ability to call a die good after only wafer probe testing – i.e., without dependence on package test or burn-in. Providing KGD is especially important as 3D and multi-chip packaging increases in use.

Testing methods need to be extended to provide high quality testing at wafer probe. Today, there are often tests that are only applied at final package test (e.g., at-speed tests, functional tests, external loopback, RF performance tests, or trimming for analog products).

As geometries continue to shrink there is a concern that voltage stress will lose its effectiveness and therefore it will become more difficult to screen for reliability-type defects with only wafer probe testing. Research should address the ability to produce reliable KGD by studying new acceleration techniques and/or quantifying the benefits of different design constraints. (e.g., low power, design with x% margin, trade off x performance for y yield, throw away x parts from uncertainty, statistical techniques for reliability, and design rules to improve reliability)

1.6 New ATPG techniques

Traditionally, structural patterns are used to test complex SoCs, but functional patterns may also be used to test and debug hard-to-detect defects. Generating efficient functional patterns is a challenging task and can be significantly expensive. Therefore, research in ATPG should focus on

improving the quality of test patterns such that the dependence on functional patterns is greatly reduced.

- New automatic test pattern generation techniques are required to target hard-to-detect failures. This entails two things: a) developing new fault models to represent failures that are being observed in some of the new technologies, and b) improved ATPG techniques to enhance fault coverage for such fault models without excessively increasing the pattern counts. In addition to defect screening, these new patterns must also assist in diagnosis and failure analysis.
- New automatic test pattern generation techniques are required to target hard-to-detect failures while still guaranteeing high fault coverage and low pattern count. In addition to defect screening, these new patterns must also assist in diagnosis and failure analysis.
- In the past, the introduction of new fault models directly translated into additional patterns that are a result of targeting such faults during ATPG. Consequently, the pattern count increases as newer fault models are expected to improve the overall defect coverage. Moving forward, ATPG techniques should be improved to develop compact pattern sets that would provide a robust coverage of not just a single fault model but a variety of fault models thereby improving the overall defect coverage.
- As designs are getting larger but time-to-market is getting shorter, more performance and memory optimization from test generation and fault simulation are needed. Research areas are optimizing test generation/fault simulation for multi-core microprocessors to use more parallelization, and use of SAT algorithms in conjunction with ATPG for test generation, especially to address hard-to-detect faults, timing constraints during test generation, and test compression.

1.7 Pattern type effectiveness, optimization and selection

Methods are required that optimizes test pattern effectiveness given test time and test data volume constraints.

The number of test pattern types and methods has continued to increase over time but the acceptable amount of time and patterns used to test each die have not increased at the same rate, if at all. In particular, recent years have witnessed the introduction of several competing at-speed test methodologies such as faster-than-at-speed testing, tests generated using shortest path information, K Longest paths, and other small delay defect test methods which compete with traditional transition fault and path delay testing methods for test time. Furthermore, there are multiple clocking strategies which can be employed including tester-based, PLL-based, launch-from-shift, and launch-from-capture. Bridging fault tests are starting to see more attention and interest, and again there are many methods for generating the fault lists and tests and merging them with the existing test suite already used in production tests. And bridging tests are just one example of the more general class of defect-driven test methodologies. Research is necessary to develop methods for trading off test time and test type to optimize the test strategy for a device given its performance, power, cost, and other product requirements, tester requirements and limitations, and defect paretos for the technology in which it is implemented. As in previous sections, it is very desirable to verify as much as possible the work results and outcomes on actual production silicon data and devices from a member company as opposed to mere fault simulation exercises.

2. Yield Learning and Improvement

Recent advances in process technology and integration have been accompanied by challenges in ensuring reliable systems with predictable and desirable yield. New generations of process nodes have proven to be more challenging to enable high yield than previously expected. The high cost and cycle time associated with physical failure analysis (PFA) of ever smaller geometries necessitates better failure isolation and more knowledge about the failure mechanism prior to performing PFA. Tools that can analyze, learn and draw conclusions from volume test data have advanced in the recent years and are ripe for exploiting for volume diagnosis.

2.1 Diagnosis and failure isolation for defects in digital systems

Test results from wafer sort are used to perform yield analysis to locate failure causation. Despite recent progress in isolating candidates for failure causation, in recent designs, the resulting candidate set is still far too large to perform probing/imaging on all such candidates for failure analysis. High-resolution failure isolation techniques in the presence of compression and/or BIST hardware, as well as techniques that leverage layout-vulnerabilities (provided or learnt) to identify defect-prone topologies are needed. Hierarchical methods that can aid various degrees of isolation at each level of design hierarchy are also needed.

2.2 Diagnosis and failure isolation for defects in mixed-signal systems

Isolation of failure causation in mixed-signal systems, such as high speed interfaces, is needed due to their recent percentage area increase in SoCs and their limited controllability and observability in silicon. BIST methods and non-intrusive observability schemes to improve diagnosability are needed. There is also a need for automation to analyze layout structures, trace back from failure observation (which could be a violation of an analog specification as in the case of an undesired transmitter output swing or a digital specification such as an erroneous sampled value at the receiver during loop-back) and perform cause-effect or effect-cause reasoning to identify either failing modules and devices. Methods to locate defects that are worsened by marginal dies and conditions are also needed.

2.3 Structural and functional test generation to aid diagnostic resolution

Methods to generate test stimuli that can effectively narrow down the failure causation candidates are needed. Tests can be functional (instructions/microcode), BIST-based, or structural using scan, or other DFX mechanisms for mixed-signal systems.

2.4 Statistical techniques to aid volume diagnosis

The pass/fail and specification measurement results from testing a large volume of dies during wafer sort provide a rich source of data for failure isolation and understanding. This data, coupled with the nature of tests applied, and the circuit and layout topologies targeted by the tests, can be analyzed statistically to extract and categorize failure patterns across dies in a wafer, wafers in a lot, and lots in a fab, to isolate different failure mechanisms, before a deep-dive on individual dies are attempted. Research is needed to understand effective ways to exploit diagnosis data in conjunction with data from design, simulation, silicon characterization, metrology, defect inspection, process equipment history, physical failure analysis results and other sources of process data.

2.5 Systematic defect modeling and test

Defects in future deep submicron (DSM) silicon scaling are trending toward more systematic failure mechanisms (versus random). Fault models and test generation methods should be enhanced to ensure high coverage of systematic defects. The occurrence of systematic defects needs to be recognized and flagged so that corrective measures can be taken.

Defects in future DSM silicon scaling are trending toward more systematic failure mechanisms (versus random) for reasons which include advanced lithography methods. Process-design interaction resulting in differences in systematic defects on products with same/similar layout rules needs to be understood. This is important since achievement of high yield on a product does not guarantee similar yield of another product/derivative on the same process. Research would be valuable into understanding and addressing systematic defects. The ability to rank design for manufacturability (DFM) checks to establish their relative importance in terms of the avoidance of time zero yield or longer term reliability losses in a given technology is of particular interest.

3. Analog, Mixed-Signal, and RF/High Speed Test

3.1 Metrics, models and methods for high speed I/O and analog test

With increasing integration of diverse analog components on a single die including several LDOs, PLLs, sensors, different high-speed communication interfaces, baseband, RF functional blocks and even embedded memory control units with nonvolatile memories, the proportion of area occupied by analog circuitry is significantly increasing and controllability is decreased.

To ensure desirable outgoing product quality at an affordable cost, it is essential to test this circuitry adequately to address both defects and marginalities. There is a need for usable and automated metrics and methods to gauge the quality of test stimulus for testing these circuits in terms of their ability to identify and quantify deviation from normal functionality or to systematically generate tests to target specific hardware vulnerabilities. Failures that can result due to unexpected/undesired process excursions should be addressed in addition to those caused by hard defects, and unified metrics that can enable comparison of test quality in terms of coverage of both these types of failures are needed. The need for new techniques for testing unidirectional interfaces are becoming more important given the increasing need for expensive test equipment in the absence of better methods. Metrics and models are needed at a level of abstraction that is adequate to capture a circuit's deviation from normal functionality, and at the same time not necessitating methods that are impractical due to reasons such as excessive simulation time. Design-for-test methods are needed that enable controllability and observability of deeply embedded analog modules. Due to falling product average selling prices, envisioned solutions should comprehend and minimize test cost. Techniques are needed that enable testing of analog front-end through digital interfaces thus lowering test cost through use of less expensive digital testers. The integration of embedded MCUs with NVM into analog/mixed signal devices gives the test technologies a higher degree on opportunities in respect of BIST but also a higher degree on complexity when considering the software dependency of test results.

3.2 Metrics, models and methods for RF test

RF test can be expensive compared to digital and mixed signal devices. To overcome this disadvantage there are few volume production-worthy test techniques published and accepted industry-wide. Alternative, alternate, loop-back techniques have been published along with some BIST and BIT techniques, but not implemented as a standard RF test technique. This area is in

need of new ideas on low cost test implementations. A theoretical and practical evaluation of the strengths and weaknesses of the proposed techniques will be required to demonstrate the advantage when comparing with established traditional RF test techniques. Parallel test techniques that reduce test time to test/measure front-end specifications are needed. Development of CMOS processes with smaller feature sizes are enabling circuits in the high GHz range which cannot be tested with the traditional commercial ATE. Also these feature sizes enable the high integration of a SOC with a limited test access to specific circuits. To enable cost-effective testing of such circuits and to overcome the limited observability model-based test and characterization approaches are areas that can be pursued.

3.3 *Fast tuning calibration and repair (manufacturing test, in-field, etc.)*

Analog circuits on silicon are characterized by their increased sensitivity to process drift. A large proportion of silicon failures are usually attributed to circuit parameter changes due to process drift rather than just gross defects. Analyzing circuit behavior during the pre-silicon design phase for different circuit parameter combinations over a wide range of process variations at a desired accuracy is usually expensive and impractical due to excessive simulation time. This necessitates the need for automated design-for-test-and-validation strategies to be used after first-silicon during bring-up (post-silicon validation) and during HVM (high volume manufacturing) test, that allow enough granularity of access to enable circuit parameters to be tuned in silicon to meet desired specifications, and not expensive in terms of power/performance or test cost. “Self-repair” and “self-calibration” schemes during device lifetime, and test strategies to predict the potential risk associated with these self-repair and calibration algorithms are needed. Test strategies for these autonomous systems, and a prediction what kind of self-repair and calibration will occur, and their limits, are needed.

3.4 BIST/BIT techniques for analog/mixed signal

Aspects to investigate include: (a) What instrumentation on tester can be incorporated on-chip as test infrastructure IP module? (b) How can such a module be re-used across different functions to be tested? (c) Can such modules be generated / created from programmable specifications for different test requirements? (d) How can software BIST be applied to analog / mixed signal circuits and what are the parameters / metrics for test and evaluation? (e) How comprehensively can BIST supplement conventional tests for test and calibration?

3.5 Coverage metrics for analog mixed-signal systems

Analog/Mixed signal test is still considered expensive when comparing to digital test; in addition a commonly accepted definition of test coverage is outstanding. Every experienced analog/mixed signal test engineer will be able to show examples when a device just failed during a input parametric window like failing within a band of temperatures within the specified range, failing for certain voltage ranges even not at the min/max limits or even when changing the startup routine like voltage slopes or start voltage. Coverage definitions for these conditions will need to be developed, verified and published.

3.6 Analog device reliability under stress

There is a need to improve the quality of burn-in and stress testing of analog/mixed-signal circuits to prevent infant mortality failures at the customer end. Methods and metrics to define the relationship between stress type and expected failure duration, and estimation of their satisfaction with a given test suite are required. This is particularly important since layout topologies and regions of device operation in analog circuits can be different from those in switching circuits.

The need for lifetime defect-free devices is growing. This trend started with the quality requirements for defense/space and medical applications and started to commercialize with the quality needs defined by the automobile industry. For this kind of devices special test coverage needs to be defined and developed. Typical for these devices is not only to have zero DPPM at the factory but also a need to guarantee fail free operations over the entire lifetime. Special test strategies need to be developed to predict potential fails. Though advances have been made on statistical methods like outlier control, these will need to be supplemented by electrical tests which lets predict defects during normal operation even for the case that the device is within specification at time zero.

Strategies for lifetime zero DPPM devices include from testing for outliers, reliability defect modeling and testing, self-repair and redundancy. Accelerated stress test above extended temperature and voltage could also be an area for research. This topic can also be expanded to test for time dependent defects, testing for trapped charges, NBTI, etc., and not limited to oxide defects.

4. High Level Test, Diagnosis and Repair

4.1 System-level test, debug and correlation to tester

The complexity and heterogeneity of components within a system makes it mandatory to develop good test techniques to catch possible failures before it is shipped. Even though individual components may perfectly pass manufacturing test, when they are put together these components (along with their interfaces) must again be thoroughly tested. Structural test methods used for system test rely primarily on BIST. The industry needs improved system-level BIST solutions that guarantee good outgoing quality at the system level. In addition to logic BIST, other solutions include “functional-BIST” and broader use of embedded test structures at the system level. Improved BIST solutions should focus on reducing or eliminating the shortcomings of logic BIST (including problems of test point insertion, elimination of unknown states (Xs), and failure diagnosis) and make its use friendlier to design and test engineers. This would ease adoption of such a technology and help the industry maintain and predict the reliability of complex devices and systems both post-manufacturing and in-field.

Currently functional test generation tends to be ad hoc and there is no systematic coverage metric to ensure test completeness and to ensure high quality test selection. Such a coverage metric, preferably computed using less computationally expensive high-level simulation methods is needed.

4.2 In-system test techniques for critical applications

(a) While modular logic BIST and memory BIST are well investigated and well applied, there is a need to stitch together these modular solutions at the chip and system level. For example, how can the overall chip and overall system be completely tested in minimal time? (b) Is there a need for a system level test scheduler which can help stitch / create an optimal (compressed) test schedule for various components, for a given set of offline and online test requirements, depending upon which set of modules can be tested concurrently, and which of them cannot, and depending upon whether the tests must be run without being interrupted (start to end) or in interrupt mode (halt-resume)? (c) How adequately can such structural techniques be used to guarantee system correctness? Where / how should they be supplemented with system tests? (d) How is the quality of in-system test measured in terms of coverage, detection latency, robustness, etc.?

4.3 Efficient test and diagnosis of macro systems – cloud and data centers

The emergence of large cloud compute and data centers has created a huge demand for efficient test and diagnosis techniques for these large systems. Currently, there is lack of good diagnostic methods to isolate failures inside a system to a particular component and, as a result, good components get shipped back to the IC manufacturer for debug. This results in an expensive and unnecessary debug process. Hence, there is a need for models and methods that nclude test and debug strategies that span the software/hardware stacks to enable isolation of failure to either a software (application layer, OS, firmware) or hardware cluster/component (such as a processor or storage module) in a system environment without compromising intellectual property and security. Permanent failures at the end-customer can occur prior to the end of the guaranteed life-time of a product due to device degradation (e.g. aging NBTI, electromigration) and infant mortality (due to ineffective burn-in). These are issues that cannot be resolved with a time zero manufacturing test. These necessitate in-the-field test and repair strategies - either concurrent (on-line) or off-line self-test, diagnosis, and correction. Notable characteristics of such failures are that faults are not transient (rollback solutions are not appropriate) and manifest gradually (hence degradation can potentially be tracked). Strategies that address such failures need to comprehend their sensitivity to use conditions.

4.4 Economics of BIST techniques for SoC

Today, BIST implemented discretely for logic, memory, analog, and mixed-signal components. BIST is not used to eliminate significant test cost components. For example, an SOC may implement various BIST techniques, but still require scan, ATPG, functional testing, etc. Hence BIST is seen as an added cost. From an economic standpoint, one must look at the factors that contribute to the total cost of the product and assess if the addition of certain BIST features to the design will reduce the overall cost or improve quality. Proper assessment of these type of economic decisions may need to take into account the life cycle cost aspect of the SOC.

5. Post-Silicon Validation

Post-silicon validation of an integrated circuit is the process of validating silicon over several iterations with the goal of qualifying the product for manufacturing test. The goal of these iterations is to refine the design and process in order to eventually qualify the product for high volume production. The duration of each iteration and the number of iterations have to be minimal to avoid delaying the time-to-market of a product. In contrast to manufacturing test, silicon validation is characterized by the following: (a) only a small sample of dies drawn from a variety of fabrication environments are analyzed, (b) the duration of analysis for each iteration is in the order of days compared to manufacturing test where each die has to be tested in seconds – thus allowing for significantly more test stimuli to be applied without concern for test volume (c) use of external instrumentation is allowed to increase the controllability and observability of silicon to facilitate debug, and (d) performance of dies in high volume has to be predicted by analyzing only a small sample of dies. Both functional bugs and electrical bugs are to be debugged and fixed. Silicon validation occurs on both on a tester and a system (board with limited OS) platform.

5.1 Efficient system-level functional debug

Once a bug is found, classifying it as a functional vs. marginal bug is relatively straightforward in silicon, based on the volume of its impact. However, functional bugs are notoriously hard to detect due to the absence of a “golden” model since the issue is present in both RTL and silicon. Silicon provides an indication of failure through either an application crash on a system, a blue screen, or the

failure of a self-checking test. Debugging such failures involves working backwards from the failure observation point, which is usually a corrupt state, and tracing it back to a control flow violation or a data-path error. Methods to characterize a design and automatically generate properties (e.g. control flow paths, invariants) that can be potentially checked for violation during simulation, or using DFX hooks in silicon, to explain the failure, are needed. High level surrogates such as virtual platforms that can emulate an entire system with in-built flexibility in level of detail and hierarchy that is captured, should be investigated as an aid for debug and diagnosis. Once a bug is root-caused, automated methods to create compact test stimuli that can reproduce the bug are needed. . Methods that can create a structural test to recreate a functional failure are needed. Further, design-for-debug methods that can non-intrusively aid in improving controllability and observability are required. Methodologies developed should demonstrate scalability to a big system such as a microprocessor (e.g. OpenSPARC) or SoC.

5.2 Silicon validation of mixed-signal systems

SoC products have several analog/mixed-signal components (PLLs, sensors, phase-interpolators, amplifiers, DAC/ADC etc.), often in high speed interfaces such as DDR, USB3, PCIE3, integrated on to the die. The performance of these components is sensitive to layout topologies, process changes, voltage fluctuations, and other environmental factors like temperature. Ensuring their correct operation in high volume production requires adequate validation pre- and post-silicon. Since post-silicon validation is performed only on a small sample of parts, predicting the quality of the ensemble from the sample is a challenge. Analysis and simulation methods to trace back an undesirable deviation from an expected output specification, to identify the analog or digital component that should be fixed, are needed. Debug methodologies should be demonstrated to scale for mixed-signal systems such as a USB3 interface.

6. Test and Power

6.1 Test and power management, including low power devices and low power modes

As the need for mobile applications is on the rise, there is a huge surge in the demand for low power devices. Power consumption is often seen as the limiting factor for the amount of functionality one can put on such devices. There has been significant progress on designing power-aware systems that adopt a variety of design techniques to limit power consumption during operation. However, the shift and capture operations during scan test can significantly increase the stress on such devices. The challenge is to mimic the power profile of the functional mode of operation during test. Research opportunities include:

- DFT for power management methods and tools for understanding power density
- cross-chip power variation and temperature variation during testing methods for stressing and detecting defects given power boundaries
- effective design of tests that would help validate the different power modes and the transition between them

Many chips incorporate various power-saving features such as multi-Vdd, multi-frequency, sleep modes, state retention registers, etc. How do we effectively test those chips in all these modes of operation without substantially increasing test cost? How do we classify chips that pass all the tests but fail to meet their power goals? How one can ensure a device being operated closely to the functional mode of operation during test? Is there a notion of “power binning” similar to frequency binning. Are there certain types of defects that attribute to these power-failing devices? Measuring power occurs over many clock cycles, so unlike timing, it is hard to pinpoint the specific part of the design that might be causing the problem. What is the appropriate level for doing debug/diagnosis to understand the cause of power-failing chips and to identify design/process trends that could be

corrected?

6.2 Test for power delivery effects

Power delivery is a function of multiple factors, including voltage regulator module, motherboard, packaging and on-die parasitics, power gating, multi-cores, clock-gating and other power mechanisms. It is increasingly necessary to have test strategies that ensure that defects or marginalities in these multiple mechanisms, together or individually, do not cause a functional failure. Manufacturing tests often do not have the same conditions to mimic the power profile compared to when the DUT is operating within a system. There are opportunities to propose new methods that would help test the devices under conditions that would resemble the functional mode of operation. Testing mechanisms may include creation of targeted functional/structural tests that stress power delivery vulnerabilities by exciting various scenarios (e.g., low and high frequency power droop, IR drop etc.), power delivery testing state synthesis, and power delivery failure diagnosis.

6.3 On-die test structures and instrumentation for data collection including thermal

The need for test-structure-based on-die data collection is driven primarily by (1) within-chip variation that limits the representativeness of scribe-line structures and (2) need to monitor chip behavior during operation and over lifetime. Complicated design-process interactions make product-based learning attractive, but test structures are also needed to provide additional data for both post-silicon validation and yield-learning. Specifically, improvements are needed in structures that provide manufacturing process information, especially those that can distinguish the effects of different process parameters, those that provide run-time voltage and temperature information, and those that monitor reliability-related degradation.

6.4 Testing low power management structures and high voltage/current devices

With the increasing number of features in a device, significant power management circuitry is being added to control power dissipation during functional operation. This needs to be tested as well. Research opportunities exist to determine the failure mechanisms for these structures, and to develop specific tests to target these failures and methods to integrate these tests with patterns for the remaining logic. On high voltage/current devices side, wafer processes are in development to allow integration of circuits for the voltage range of up to 1kV. It will be difficult to supply in a safe, cost efficient way these high voltages to a device under test (DUT). Research topics to overcome this difficulty might include BIST techniques but also DUT internal generation. A demonstration of the proposed technique would be beneficial to show the advantages and limitations

7. Testing for Resilient/Adaptive Systems

7.1 Testing of resilient features

Resilient features are on-chip structures which can be used to configure the product to work around patent defects or confer tolerance to latent defects. These structures span a wide range of circuits and architectures, including fuses, redundant memory elements, architectures capable of operating on reduced numbers of logic elements like CPU cores or graphics components, error-detection and correction and retry schemes for hard and soft errors, and the sensing and control circuitry for adaptive designs. Like every other circuit, these structures must be themselves tested and characterized, though these circuits present unique testing challenges beyond standard logic and memory elements, including temporary configurations (for fuses), soft-repair vs. hard-repair

validation (for memories), combinatorial explosion of partially deprecated feature variants, the need for error injection to test recovery circuits, and analog stimulus for sensors (such as voltage or aging monitors).

7.2 Non-deterministic device behavior: test and run time availability

Non-determinism is incompatible with traditional cycle-accurate automated test equipment, but is nonetheless becoming typical on modern SoCs. Several new I/O protocols are non-deterministic, as are the standard methods to avoid metastability in clock-domain crossings (which are commonplace in highly integrated devices). Fine-grained power gating and power-state management can change the configuration of a device and its execution profile during test and normal operation. Adaptive designs (see 7.3) take this notion even further with architectural features which can perform state rollback and pipeline retry based on events at arbitrary times during execution. The result is that test patterns, particularly functional patterns which execute in mission mode, must either prevent or be tolerant of non-deterministic response. The former may compromise coverage questions, the latter presents pattern and ATE interface challenges.

7.3 Testing for aggressive/adaptive designs

Establishing the operating point of an SoC, or portions thereof, is no longer an event done once on the test floor. Instead, on-chip sensors are used to detect the workload, voltage, temperature, and timing margin of the chip as it operates and dynamically modulates power supplies, clock frequencies, thermal control, and workloads. Not only does this approach require careful testing of the (interrelated) feedback control system components, it also runs counter to the traditional ATE-centric method of measuring at fixed corners to verify performance parameters and could introduce a much larger space over which the device must be tested. The removal of excess margin represented by traditional guardbanding increases the risk of exposure to subtle defects, necessitating both higher coverage and better correlation between structural and functional test modes.

7.4 Leveraging resiliency techniques for efficient system validation

The process of validating system hardware requires exploring the operating space of the design in all its configurations, both static and dynamic (i.e. those set at the factory based on test results as well as those resulting from the device's sensing and adapting to its conditions during operation and over the installed product's lifetime). Some resiliency features will manifest themselves simply as a larger number of static configurations to be validated, while others will require potentially complex error injection mechanisms to activate and test the operation of the feature. Correspondingly, resiliency feature design should take into account how the feature can be selectively controlled in a validation environment to minimize the impact on lab resources and engineering time.

8. Test for New Applications and New Technologies

8.1 Test and security

Computing products developed today are designed with several operational protocols and implicit assumptions on constraints that need to be met at each layer of abstraction. As an example, a processor provides access to the OS to certain features in protected mode. While these modes are usually validated for correctness, mechanisms are needed to ensure that their invalidation due to unforeseen device operation does not render the hardware, and the information it contains, vulnerable to exploitation. Furthermore, techniques that can analyze a system that could become

vulnerable to exploitation due to hardware defects or marginalities (exposed by over-clocking for example) are needed.

There also exists a class of products that requires design and test information to be maintained in a secure way, e. g., devices that are used in cryptography or defense or similar applications. Many of those same products also require very thorough testing. Traditional solutions such as full scan can provide a high level of coverage but also render the product vulnerable to compromise of its internal structural details through reverse engineering. Logic built-in self-test (BIST) is often used to either supplement or replace conventional externally-based tests, but then diagnosis becomes more difficult. The primary objective of research in this area should be the development of test methods which maintain product details securely, but afford both high levels of defect coverage and very good failure diagnosis.

8.2 Testing and DFT for 3D

3D (silicon layering with through silicon vias or TSVs) appears to be a leading contending solution for silicon integration in high performance and/or low footprint applications. 3D technology is very much in flux and hence TSV technology is equally in flux. A research challenge is to understand defects inherent to TSVs and develop methods to detect these defects. Not all 3D/TSV solutions will require probing or can be probed because of pristine surfaces needed for subsequent bonding or the TSV technology being implemented.

Potential solutions include skipping wafer test or design level assembly. Research in this area should address test methods and infrastructure which minimize yield loss issues due to reduced or eliminated test steps and maximize test coverage using existing accessible signals such as those on the periphery of the stacked devices. Researchers should assume that mixed technologies (digital, memory, and/or analog) may be stacked.

8.3 Test for multicore chips

Single die with multiple instantiations of IP are increasingly common. Test data volume is a frequent problem in these types of devices. Some historical methods include pipelining and/or broadcasting inputs and collecting and/or comparing outputs. However these may not be the optimum solution to scale to very large arrays of IP. Opportunities could include more capable on-die test management such as an IP core being capable of directing other tests. Solutions should comprehend not only test but also debug and data collection.

8.4 Test for current/emerging technologies

Some new or emerging technologies are presenting increasing test challenges. The use of various forms of non-volatile memories (NVM) is on the rise and their testing can be costly, especially for retention. The failure modes of NVM devices are fundamentally different from conventional CMOS memories (SRAM, DRAM, eDRAM, etc.). Therefore understanding the failure mechanisms in these emerging memory technologies and developing appropriate fault models is crucial for being able to design efficient testing techniques and structures. Retention failure and retention-time testing are becoming critical for semi-nonvolatile devices in cache applications. Efficient high volume retention time test methods to ensure the average endurance of a cell are needed. The stochastic nature of failures in some NVM devices (e.g. spin-based devices) in contrast to deterministic electrical charge leakage in DRAM based devices makes the retention time testing costly and challenging. Furthermore the sensitivity of NVM devices to new pattern dependent failure requires more efficient test pattern generation. The above factors necessitate re-evaluation of traditional memory test,

repair, and yield improvement techniques to these technologies, and development of new design-for-test and design-for-yield strategies.

MEMS devices are also more prevalent and often require fundamentally different test methods than have been developed for purely electronic systems. Manufacturers of high speed data communications devices are looking to increase speeds and lower power through photonic connections, either integrated or fully embedded, and again, new test methods will need to be developed to address this fundamental technology shift. In general, changes in materials and in the building blocks for electronic systems must not result in poorer quality due to a lack of adequate manufacturing tests.