Research Needs for Extending CMOS to its Ultimate Limit
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2002 CMOS Extension Task Force
SRC Nanostructure & Integration Sciences and Materials & Process Sciences
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Front End Processing

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Introduction

The semiconductor industry has sustained a steady scaling rate of integrated circuit technologies over the past four decades. Despite periodically expressed skepticism, Moore's Law [1] has prevailed, with the linear dimensions of digital transistors reduced by one half every 2 – 3 years while still improving their current drive capability per unit length. As a direct result of this scaling process, the transistor propagation delay in digital CMOS circuits was reduced by one half over a comparable period, while density increased by a factor of four. Both trends led to today's GHz-speed PCs, the microprocessor engines that contain tens of millions of transistors of 100-nm-range dimensions and dissipate power in excess of 10's W/cm^2.

As inter-atomic distances are approached, understanding and modeling the complex operation of nanometer-size transistors become extremely challenging to the research community. In addition, new concerns arise about whether the scaling will continue at the same rate, and whether the efforts needed to sustain the process will be worth doing from a business perspective.

In a previous document, issued in 1999 for the SRC research cycle that ends this year, the Research Needs and Gaps were presented for extending CMOS technology to the 35-nm node. With highly creative discoveries and developments of new materials, processes, and transistor structures, many of the gaps initially identified have been filled. At the present time it has been clarified that the potential "Red Brick Wall" of the 100-nm technology node, defined in the 1999 edition of ITRS [2], can be reached as early as 2003. The near-term target has been moved to 65

[1] Includes input from 10 organizations (Agere, AMD, IBM, Intel, LSI-L, Motorola, National, TI, UMC and ISMT)

nm, expected to be reached in 2007. The long-term target is being moved to the 22-nm node, which is expected to be reached no later than 2016. It is the long-term portion of the 2001 ITRS [3], past the 65-nm node, that is being addressed, in terms of Research Needs and Gaps, in this new SRC research period. More specifically, this research period is addressing the 2001 ITRS requirements for the 45- to 22-nm nodes, which are broadly believed to be reached between 2010 and 2016.

The purpose of the present document is to propose an updated R&D strategy and the associated Research Needs related to extending CMOS to the 22-nm node of the current ITRS. It is particularly intended to address the Research Needs associated with the front-end aspects of extending CMOS technology. Areas covered include transistor structures, front-end materials and front-end processes along with their characterization and modeling/simulation infrastructure. Areas not covered include lithography, back-end processes, circuit architecture, design and test. Although these are all very important areas that need to be addressed in extending CMOS, they are beyond the scope of the ADT and FEP thrusts. Also, of the two Grand Challenges defined in the 2001 edition of the ITRS, only the first one is being explicitly addressed, i.e., Enhancing Performance. The second one, Cost-Effective Manufacturing is known to be present, but is not addressed explicitly.

Applications and Roadmap Drivers

Potential application drivers for the roadmap period of interest include personal computers and digital assistants, speech recognition machines and real-time language translators, very-high-resolution video encoders, digital communication products, quantum-mechanical device simulators and petaflop computers. While most of the application drivers listed include various combinations of digital, memory, analog and RF modules, the current document will concentrate on the Research Needs for developing digital modules. Research Needs related to analog, RF and Mixed Signal technologies were identified and reported in an earlier report prepared by the Mixed Signal Task Force (http://www.src.org/member/sa/nis/futures.asp).

The 2001 ITRS Roadmap for FEP and PIDS addresses technology *needs* required to extend CMOS to the end of the Roadmap, i.e. to the 22-nm node, but says little about specific technological *solutions* or related research required to achieve these needs. This document is intended to identify and prioritize avenues of research required to identify and/or devise various

candidate solutions proposed to address the technology needs. Consequently, our starting point for this first version of the Research Needs document is the 2001 ITRS Roadmap.

Scope and Technology Requirements

The scope of this document will be limited to those Research Needs related to extending front-end fabrication of CMOS from the 65-nm node (development) to its ultimate limit at or beyond the 22-nm node. The present Research Needs document focuses on "CMOS Extension" technologies, i.e., to those technologies that, while highly innovative, are still based on the CMOS logic gate as the main building block of digital products. Research Needs related to "Beyond CMOS" technologies will be addressed in a separate document being prepared concurrently. Further, the present document covers the Research Needs of front-end processing and materials, and device structures, along with the supporting characterization, modeling and simulation techniques. The research needs associated with lithography, back-end processing, design, and test are beyond the scope of this document.

The technology requirements that historically have been driving CMOS – integration, functional density, clock speed, and power dissipation - remain unchanged. The major technology barriers to scaling CMOS and improving performance remain - scaling power supply voltage, sustaining low leakage current, increasing drive current, etc. However, there are qualitative differences between the role various barriers played in the past research periods and the current one as described below. Also, the weight to be placed on filling various gaps is different in the current period.

Current Research Needs

The Research Needs of the current research period are organized into six major categories, as shown in Table 1: (1) CMOS Compatible Device Structures, (2) Gate Stack, (3) Junctions and Contacts, (4) Substrate Engineering, (5) Modeling and Simulation, and (6) Characterization Development. Of these, five were included, with slightly different titles, in the 1999 Research Needs document. The "CMOS Compatible Device Structures" is new and significant. It defines a category that, although implicit in the previous document, has a special importance in the research period being addressed.

Historically new process generations have been limited by the lithographic capability to print small patterns the size of the minimum gate length required by the new technology. The role of

lithography tends to be different in the end-of-roadmap processes, in the sense that availability of required fine lithography remains a necessary, but not sufficient condition for assuring feasibility of a new process. This is because nanometer MOSFETs are no longer scaled short-channel devices with long-channel behavior. They are true short-channel devices, the structure of which has to withstand drain-induced barrier lowering (DIBL, ultimately leading to device punch-through) without exceeding the maximum source-drain leakage current that can be tolerated by the application. For example, the double-gate MOSFET, which emerged in importance during the previous research period, reduces DIBL beyond the limit where the halo-implants of the sub-0.25-μm processes ceased to do the job, because of the symmetrical structure of its transverse (gate) field. Approaching the 22-nm technology node, other device structures may be needed where a double-gate MOSFET may no longer withstand punch-through. Similarly, new device structures may be needed to overcome fluctuation problems associated with the small number of dopants in the active region. While the new devices are expected to be highly innovative, they still have to satisfy the fundamental criteria of functional scalability and economic viability.

Another qualitative difference from the previous periods is the increased emphasis on new materials. This is present in each of the Gate Stack, Junctions and Contacts, and particularly in the Substrate Engineering categories for the following reasons. When the new device structures provide virtually all that can be expected from the materials in current use, i.e., when the "material-limit" performances are reached, additional performance boosts can only be expected from new materials with superior electronic properties. Such properties include high mobility (channel), high dielectric constant (gate stack), controllable work functions (gate electrode), or low-resistivity (source/drain and associated contacts). Such challenges are far more complex than those involved in the creation of bulk materials with specified properties. The materials being sought in this program are intimately integrated constituents of very small (~ 10-100 nm linear dimensions) structures that are batch-processed at wafer level and must be optimized for well-defined device-level electrical performance.

Yet another qualitative difference from the previous periods is the emphasis on material and structure characterization, which is included in the Characterization Development category. In addition to the 2D and 3D dopant profiling, which has remained essentially unsolved over several research periods, new metrology needs are being formulated. These include metrologies for high-spatial-resolution strain measurement of patterned surfaces, dopant profiling and dose monitoring in small area and non-planar topographies, and characterization of surface mobility in

new substrates such as Si/Ge, etc. Similar requirements for material characterization are in the Modeling and Simulation category, with the understanding that the new modeling and simulation tools have to be provided with the supporting database and model parameters for the materials involved.

It is also important to realize that most of the industry has not yet embraced any of the advanced device structures that have been demonstrated at the research level. This is due, in part, to the difficulty in transitioning existing design infrastructure as well as the uncertainty created in the manufacturing environment.

Finally, continuation of the trend of performance doubling every 2 - 3 years may well be limited by power dissipation. While ultimately the total power dissipation may be managed by forced cooling, the passive power dissipation through drain-to-source and gate-to-channel leakage currents will become increasingly detrimental to circuit operation and will limit overall performance. The unavoidable leakage current limitations are expected to invite new circuit design options. Such options are acknowledged, but not addressed in this document, as they are considered to be outside the scope of the ADT and FEP thrusts.

The "Process Integration" category formerly present has been excluded this time with the understanding that member companies will integrate internally, into their particular technology infrastructure, new process or device architectures they choose for commercialization. Implicit in the above is the requirement that proposals of new process and device architectures will still have to be conceived consistent with satisfying fundamental "integratability" criteria. For example, a process architecture that restricts temperatures to below 500 ^{o}C and uses implanted dopants would need to address low temperature activation of the dopants.

Research Needs identified for the current research period are organized into six major categories and are listed in Table 1. The topic names are self-explanatory in the context of an abundant literature dedicated to CMOS scaling [4-20].

Research Strategy

The strategy proposed to address the above-defined Research Needs calls for two major parallel research approaches leading to MOSFET technology for the 22-nm node.

1. The first approach addresses non-classical CMOS transistor structures coupled with traditional materials (e.g. SiO_2 gate dielectric) and processes, or, where appropriate, coupled with new materials (e.g., high-k gate dielectrics, metal gate electrodes, etc.). These non-classical CMOS technologies include MOSFET structures such as Ultra-Thin-Body (UTB) Silicon on Insulator (SOI) (with raised S/D contacts), Double-Gate, and UTB Double Gate. Non-classical CMOS structures offer better control of short channel effects (realizing lower subthreshold slope and lower V_t), improved I_{on} via higher channel mobility, lower load capacitance and lower propagation delay time. These structures also offer lower I_{off} and lower switching energy that, respectively, reduce the need to implement a high-k gate dielectric and lower power dissipation.

2. The second approach is focussed on new materials and processes coupled with the traditional bulk CMOS transistor structure, and later coupled with the non-classical structures. Extension of CMOS to and, perhaps, beyond the 22-nm node may require a new non-classical MOSFET structure coupled with advanced materials and processes. Classes of new materials include high-k gate dielectrics, metal and mid-gap gate metal electrodes, strained silicon and silicon-germanium alloys, etc. These new materials will lower the gate leakage current, lower the gate resistance and reduce the poly-gate electrode depletion capacitance, and increase device speed through increased I_{on}.

This proposed strategy is quite appealing for two reasons. First it enhances device performance. Second it lowers the risk of achieving the 45- to 22-nm technology nodes. This is accomplished by consolidating the technology options (device structure and new materials) for the 45-nm node (the first node of the roadmap interval of interest), while allowing for possible revolutionary innovations that would ultimately break through existing barriers towards the 22-nm node.

Research Priorities and Funding Gaps

The Research Needs given in Table 1 were ranked in terms of two criteria. First, the Research Needs were prioritized according to their relative importance to extending CMOS to the 22-nm node. The question asked for this prioritization is "How important is the *knowledge* obtained, related to each Research Need, to extending CMOS to the 22-nm node?" This may be referred to as the Research Priority or "Knowledge Gap", and is given in the "Priority" column of Table 1. Second, the Research Needs were ranked in terms of their funding or "Resource Gap". The question asked for this prioritization is "Given current funding in each research area remains the same, to what extent is each Research Need *adequately funded* to acquire the required knowledge when needed?" The funding includes resources provided by SRC, MARCO, federal agencies, corporate funding, etc. This ranking is listed in the "Gap" column of Table 1. Both of these rankings are quite subjective, but they will guide SRC's solicitation and selection of only those highest quality proposals addressing only those topics most important to extending CMOS to the 22-nm node.

The importance or Knowledge Gap prioritization by the participating member companies ("Priority" column) was reasonably consistent despite the rather large differences among these member companies in terms of technology infrastructure and CMOS development strategy. The topics were ranked and color-coded into three categories of priority. The result of this ranking is represented in Table 1, where the red, yellow and white colors are assigned to the high, medium, and low priority Research Needs, respectively.

Prioritization of the Research Needs according to their funding or Resource Gaps is also shown in Table 1 ("Gaps" column), where the Research Needs were color-coded into three categories. A Research Need colored in red indicates *substantial additional* per annum funding is needed to acquire the needed knowledge within the required time frame. Yellow means *moderate additional* annual funding is required, and white indicates that the per annum funding for that Research Need is adequate to obtain the needed knowledge in a timely fashion.

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Table 1 –Research Needs for Extending CMOS
Research Prioritization and Funding Gap Analyses

Descriptive Topic	Priority	Gap
Device Structure		
SOI structures including partially depleted, fully depleted, ultra-thin body devices, etc.		
Double/multiple gate and ground plane devices		
Alternate-material MOS structures		
Device architectures for minimizing effects of statistical dopant fluctuation and layer non-uniformity		
CMOS compatible device structures		
Device architectures for solving heat dissipation in thin-body devices		
3D device architectures		
Threshold voltage control for multiple-threshold-voltage applications		
Gate Stack		
High-K dielectric gate stack materials capable of 1-nm effective inversion gate-oxide thickness		
Reliability performance for new gate stack materials including intrinsic defect density, charge trapping, dielectric breakdown, negative-bias temperature instability, etc.		
New materials for gate electrodes including metal gates with tunable work functions.		
Enhanced carrier mobility for high- K gate stacks and improved understanding of mobility effects including charge trapping, scattering, etc.		
Improved understanding of dielectric/silicon and dielectric/gate interfaces		
New gate stack deposition processes including MOCVD, UHCVD, ALD, MBE, etc.		
Improved understanding of polysilicon gate properties on high-K materials (dopant diffusion and activation, carrier depletion, etc.)		
Junctions and Contacts		
Ultra abrupt (~ 3 dec/nm), low resistivity junctions including those made by metastable activation, doped material deposition, etc.		
Extremely-low-contact- resistance silicides for S/D and gate contacts		
Contact schemes for low-contact resistance S/D and gate electrodes		
Contact schemes for ultra thin body MOSFETs, including raised S/D structures		
Improved understanding of influence of device parasitics on device performance		
Substrate Engineering		
High-mobility substrates including strained silicon and new materials on Si and insulating substrates		
Improved thickness uniformity in ultra thin body devices (<10 nm)		
Ultra-thin-body substrates (~ 10 nm) including SOI, ELO, etc.		

Control of line edge roughness for fins and gates		
Optimization of strained-Si layer structure and composition for CMOS compatibility including reduction of defect densities		
High-selectivity etching and cleaning processes		

Modeling & Simulation Development

Scalable, accurate, computationally efficient compact device models for ultra-small devices		
Modeling and characterization of dopant implantation, diffusion and activation, defect formation, strain, interface segregation, etc. in silicon, polysilicon, Si-Ge, etc.		
Modeling and characterization of electron transport in MOSFETs based on silicon and new materials including ballistic and quantum effects		
Modeling and characterization of reliability of high-K gate stacks including TDDB, CHC, etc.		
Modeling and characterization of electron transport in strained materials and ultra-thin body devices		
Atomistic modeling of materials and interfaces		
Modeling and characterization of charge trapping mechanisms in dielectrics for lifetime projections		
Modeling and characterization of dielectric deposition/growth processes in their relation to defect formation		

Characterization Development

High-spatial-resolution strain measurements of patterned surfaces		
Characterization of interface/film for leaky dielectrics including electrical characteristics, thickness extraction, mobility, etc.		
2D and 3D dopant profiling		
Measurements of gate stack thickness and dielectric constants including multi-layer and gradient effects		
Analytic interface measurement techniques		
Characterization of surface mobility in new substrates such as Si-Ge and UTB, including understanding of fundamental physical limits		
Electrical test structures for high frequency and reliability characterization		
Dopant profiling and dose monitoring in small area and non-planar topographies such as trenches, fins, etc.		
Analysis methodology for back side SiO2 interface states and fixed charges		

Priority Legend[1]

High Priority Research Topic	
Medium Priority Research Topic	
Low Priority Research Topic	

Funding Gap Legend[2]

Large Funding Gap	
Medium Funding Gap	
Small Funding Gap	

[1] There is no relative ranking. All research topics have the same priority within each color group.

[2] A critical assumption in the funding gap ranking is that current funding in these areas remains the same.