

Research Needs for Device Sciences Modeling and Simulation (May 6, 2005)

SRC Device Sciences
2005 Modeling and Simulation Task Force
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Introduction

Technology computer-aided design (TCAD) has become essential to advanced technology development, contributing to solving a diverse range of problems from equipment design and process control through to device compact modeling and design variability analysis. The complexity of a modern technology is such that it could not be successfully completed without extensive use of modeling tools in almost every aspect of its development. At the heart of technology scaling, process and device simulation has played a critical role by giving insight into the relationships between processing choices and device performance that cannot be obtained from physical metrology tools alone. Process and device simulation tools have become a key enabler for the semiconductor industry to continue to achieve increasing device density and performance with high yield and manufacturability.

The Device Sciences area of SRC has divided its modeling and simulation portfolio into two thrust areas: “Compact Modeling” and “Modeling and Simulation”. This document presents Research Needs related to the “Modeling and Simulation” thrust area, meaning the numerical modeling and simulation of front-end processes and devices for both logic and memory. A separate Task Force has been formed to address needs in the “Compact Modeling” thrust area. The SRC Device Sciences area currently funds 12 research contracts in this area, in addition to several contracts in other thrust areas that have a significant modeling component. Modeling and simulation Research Needs are strongly guided by overall technology research directions as described in an earlier Task Force report [1], and by the ITRS [2]. This document was prepared by a Device Sciences Task Force with the following contributors:

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Scope

Consistent with the strategic plan of the SRC Devices Sciences Area, the Task Force considered research needs both for Evolutionary and Revolutionary CMOS modeling and simulation. The Evolutionary CMOS era addresses continued scaling of CMOS devices down to the 22-nm node or beyond, characterized by the continued use of silicon as the channel transport material. This poses tremendous technology challenges since no manufacturable solutions exist for gate stacks and ultra-shallow junctions for sub-32 nm technology nodes. Modeling and simulation has an essential role to play in enabling solutions to be found and applied to produce manufacturable technologies, both for logic and memory applications.

As CMOS scaling approaches the deep nanoscale regime, it is anticipated that conventional silicon CMOS scaling will face fundamental limitations at or beyond the 22-nm node. In that Revolutionary CMOS era, new device architectures and process modules need to be explored that incorporate alternative channel transport materials and device structures. Modeling and simulation is needed to guide exploration of these technology options and enable early assessment of their potential to replace more conventional architectures for logic and memory applications.

At an even longer time horizon, the Exotic Technologies era considers options beyond charge-based devices as an eventual replacement for the CMOS switch. Although important as a long term strategic research direction for the industry, modeling and simulation for these technologies was considered to be beyond the scope of SRC Device Sciences research funding and so beyond the scope of this Research Needs document.

Role of the Network for Computational Nanotechnology

The SRC is a charter member of the Network for Computational Nanotechnology (NCN), an NSF-sponsored multi-university organization aiming to be the place where experiment, theory, and simulation meet to discover and exploit new scientific and technological opportunities in the nanotechnology domain. For SRC researchers, the NCN offers a web-based community where modelers and experimentalists can connect and benefit from each other's work. NCN researchers are developing simulation toolkits to accelerate the exploration and implementation of modeling ideas, and can enable online access to simulation tools through the NanoHUB web site (www.nanohub.org). SRC researchers are encouraged to partner with NCN in their research plans to benefit from the resources available there and accelerate their modeling and simulation research progress.

Research Needs

Following the structure of our Strategic Plan, the Task Force divided our assessment of Research Needs into Evolutionary and Revolutionary CMOS categories, and between process modeling and device modeling areas. Nevertheless, we strongly encourage research work to take a comprehensive view of technology development challenges and propose research work that bridges across areas to deliver fundamental understanding of the relationships between processing conditions and device performance, including coupling to experimental work. We also encourage research across the modeling hierarchy from very detailed physical descriptions through to approaches more directly applicable for industrial technology analysis. Specific needs for the Memory area and cross-cut modeling needs are also addressed.

Looking at the overall Research Needs prioritization by area, one notable outcome is the clear weighting of Evolutionary CMOS process modeling topics above other areas. This reflects our assessment that the state-of-the-art in process modeling is significantly further from current industrial needs than is the case for device modeling. Additional research investment is required to address this gap, and will also strengthen the foundation for extending process modeling into the Revolutionary CMOS regime.

Process Modeling – Evolutionary CMOS

Doping process physics for conventional and non-classical silicon devices

Modeling of doping-related processes was identified as the highest priority research area with the largest gap between research needs and current funding. At the heart of technology scaling is the ability to form ever shallower and more abrupt junctions while maintaining or increasing dopant activation so that short channel effects and series resistance can be kept at acceptable levels. Detailed understanding of dopant-defect annealing and activation remains a challenging problem, particularly with the move towards very low thermal budget flows and millisecond annealing techniques where ion implantation damage may not be fully removed. The addition of strained silicon, silicon-on-insulator (SOI), and SiGe further complicate the understanding of junction formation, amorphization/regrowth, interface kinetics, and extended defect behavior. The move towards non-planar device structures requires understanding and modeling these effects in realistic 2D/3D geometries including the influence of sidewalls and mask edges. Understanding variability in manufacture will require modeling of fluctuation effects in structure and doping.

Gate stack modeling for 0.5nm EOT and beyond

The second highest priority modeling challenge is the detailed understanding of materials and interface properties of the gate stack, aimed at structures with an equivalent oxide thickness (EOT) of 0.5nm and below. The successful introduction of high-k gate dielectrics and metal gate electrodes for successive generations of technology will require a detailed understanding of materials properties at an atomic level, allowing engineering of desirable properties such as interface state density and gate workfunction. Detailed materials understanding must be connected through to device properties such as mobility and reliability to make the overall design tradeoffs clear.

Process Modeling – Revolutionary CMOS

For the longer time horizon, the main research need for process modeling is to begin to extend the highest priority silicon areas of diffusion/activation and gate stack interfaces to beyond-silicon materials systems. Stress effects are expected to play an even larger role in such

devices. Detailed materials modeling from the atomic level up to continuum will be essential, again relating materials and process conditions to operation of the resulting device structure. Models for non-CMOS devices based on new materials heterogeneously integrated on a silicon substrate will be needed to evaluate these approaches, including understanding interface structure and its relation to device effects such as interface states and Fermi level pinning. Particular emphasis should be placed upon formation and propagation of crystal defects in these new materials and their impact on device operation and performance. Modeling of contact formation is also expected to be important because these are becoming an increasing bottleneck to device performance. Finally, the challenge of gate stack engineering will continue to be a critical need, now expanded to address high-k dielectric interfaces with non-silicon channels.

Device Modeling – Evolutionary CMOS

The highest research priority for Evolutionary CMOS device modeling is the development of robust and detailed 3D device modeling including quantum confinement, ultra-thin body, strain, and surface orientation effects. All of these features are required to understand the operation, performance, and scalability of non-planar device candidates such as the FinFET. Non-planar devices will also incorporate novel gate stack materials, so their effect on device performance and reliability must be understood. Further, understanding the electrostatic and transport characteristics of transistors consisting of heterogeneous semiconductor materials will be of increasing importance. Finally, thermal management in scaled technologies is an increasing concern made worse by the introduction of materials with poorer thermal conduction (SOI, SiGe) and the physical confinement of non-planar device geometries. Models for heat dissipation including non-classical effects are required to understand how thermal considerations will influence overall device properties.

Device Modeling – Revolutionary CMOS

For the Revolutionary CMOS era, device modeling should focus on physical modeling for transport in beyond-silicon devices for both electrons and holes to enable early assessment of their performance potential. This includes extending traditional device modeling approaches to new materials as well as developing new, efficient simulation approaches for transport in the quantum mechanical regime with a comprehensive treatment of scattering mechanisms. This

will equip us to analyze the properties of highly scaled devices, moving towards quantum-dominated structures such as nanowires and carbon nanotubes.

Modeling for Memory Applications

While there is substantial overlap between logic and memory technology modeling needs, some materials and structures are unique to memory applications. These were considered by the Task Force, but evaluated as a relatively lower priority compared to most logic technology modeling needs.

Cross-cut Modeling Needs

Some modeling and simulation infrastructure has application beyond the process and device modeling areas and so was considered as a crosscut need. The highest priority in this area is development of 3D mesh generation and adaptation in support of 3D process and device modeling. Metrology is also a critical cross-cut need where modeling has a significant role both as a recipient of metrology information and as an enabler of advanced metrology techniques through co-development of models and measurements. Metrology needs are being addressed through a separate cross-cut area at SRC, but research proposals coupling advanced metrology development with modeling and simulation are encouraged. Likewise, although compact modeling is being addressed through a separate Task Force in Device Sciences, proposals linking compact model development with physical modeling and simulation are also encouraged.

Research Priorities and Funding Gaps

The Research Needs listed in Table 1 were ranked in terms of two criteria. First, the Research Needs were prioritized according to their relative importance. The question asked for this prioritization was “Which Research Needs identified for modeling and simulation are most important to provide SRC member companies with the modeling and simulation techniques and tools needed to scale CMOS to its ultimate limits?” This is referred to as the Research Priority or “Knowledge Gap”, and is given in the “Priority” column of Table 1. Second, the Research Needs were ranked in terms of their funding or “Resource Gap”. The question asked for this prioritization was “Which Research Needs require the most additional work (beyond that work being funded at this time) to provide SRC member companies with viable modeling and

simulation techniques and tools?” The funding includes resources provided by SRC, MARCO, federal agencies, and corporate funding, and assumes that current funding levels are not changed. This ranking is listed in the “Gap” column of Table 1. Both of these rankings are quite subjective, but they will help guide SRC’s solicitation and selection of only those highest quality proposals addressing only those topics most important to producing the modeling and simulation techniques and tools needed to scale CMOS to its ultimate limits.

Table 1 - Research Needs Importance Prioritization and Funding Gap Analysis

Process Modeling – Evolutionary CMOS:

Priority Gap

Doping process physics for conventional and non-classical Si devices

SOI structures including partially depleted, fully depleted, ultra-thin body devices, etc.		
Amorphization and regrowth in Si, s-Si, SiGe, s-SiGe, SOI, including edge effects (i.e. at least 2D); prediction of interdiffusion, residual strain and (point and extended) defects		
Equilibrium and transient diffusion/activation (including interdiffusion, stress effects) in Si, s-Si, SiGe, s-SiGe, SOI including lower temperatures for high-k/metal gate flows, millisecond annealing (Flash, non-melt laser)		
Accurate and CPU-efficient 3D implant, diffusion, oxidation (moving boundary), stress with interface/strain effects		
Structure and dopant fluctuations, finite size effects		
Pattern, die, and wafer scale uniformity effects in thermal and other processing		
Models for silicide formation including interface effects on contact resistivity		
Defect formation due to stress		

Process Modeling – Evolutionary CMOS:

Gate Stack Modeling for 0.5nm EOT and Beyond

Prediction of traps, interface states, interface kinetics of high-k materials, including detailed physical modeling of materials and interfaces. Atomistic modeling of workfunction/barrier heights		
Prediction of reliability of high-k/metal gate material stacks		
Impact of dopants on metal gate workfunctions		

Process Modeling - Revolutionary CMOS

Diffusion/activation beyond Si (Ge, III-V) – interdiffusion effects, influence of stress, interface properties, implant damage including atomistic modeling connecting structure to electrical properties		
Calculation of stress distributions in novel structures (non-Si, multilayer epi, defects and dislocations, ...)		
Process modeling of beyond-Si nanowire and CNT growth mechanisms and integration schemes to Si substrates		
Modeling of contact formation (germanides, metals, ...)		

Device Modeling - Evolutionary CMOS

Models for heat dissipation in non-planar devices; effect of temperature on devices and packages		
3D quantum mechanical electrostatics/band structure and physical transport models including strain, high-k/metal gate, UTB, and surface orientation effects		
Novel modeling approaches for device variation effects (LER, RDF, ...) and noise for logic and memory		
Reliability/breakdown physics for high-k/metal gate stacks		
Effect of local parasitics on electrical performance at high frequency in device TCAD environment		
Physical models and characterization techniques for accurate 2D/3D simulation of ESD (including thermal effects) in advanced CMOS, particularly PD and FD SOI		

Device Modeling – Revolutionary CMOS

Models for heating in beyond-Si devices and methods for removal of heat from circuits		
Physical models for transport in beyond-Si devices (Ge, III-V) enabling performance prediction/analysis		
Physical models for transport in beyond-Si devices (nanowire, CNT, ...) enabling performance prediction/analysis		
Strain effects on transport in non-Si device structures		
Realistic treatment of transport through contacts (e.g. wire to tube interface in a CNT)		
Efficient simulation of dissipative QM transport, especially using a comprehensive set of scattering mechanisms		

Modeling for Memory Applications

Modeling novel processes and devices for non-classical memory applications (MRAM, phase change, ferro, nanocrystals, ...)		
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Cross-cut Modeling Needs

3D mesh generation and adaptation compatible with numerics/solvers		
Solvers and parallelization for process/device problems		
Mixed mode simulation approaches coupling numerical device models to circuit for early novel device evaluation		

Priority Legend¹

High Priority Research Topic	
Medium Priority Research Topic	
Low Priority Research Topic	

Funding Gap Legend²

Large Funding Gap	
Medium Funding Gap	
Small Funding Gap	

¹ There is no relative ranking. All research topics have the same priority within each color group.

² A critical assumption in the funding gap ranking is that current funding in these areas remains the same.

References

- [1] “Research Needs for Extending CMOS to its Ultimate Limit”, 2002 CMOS Extension Task Force, Semiconductor Research Corporation, November 2002.
- [2] International Roadmap Committee, *International Technology Roadmap for Semiconductors 2004 Edition*, ITRS, Austin, Texas, 2004.