Research Needs for Extending CMOS to its Ultimate Limit
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Introduction

For years, while the semiconductor industry has been projecting Moore's law and performance scaling to upcoming CMOS generations, the industry has also been warning about "Red Brick Walls" of processes, materials, and physics which may block this seemingly unstoppable path to smaller, faster, cheaper devices and circuits. A first "Red Brick Wall" was considered to be limitations of optical lithography while a second "Red Brick Wall" was considered to be limitations of transistor scaling and performance arising from basic physics associated with conventional silicon CMOS designs. While optical lithography has continued to enable smaller devices and higher packing density, transistor scaling has in fact experienced a slowdown, for the first time in history. For example, scaling of the transistor gate dielectric thickness slowed from the 90nm to the 65nm technology node, due to excessive gate current concerns, with the gate dielectric thickness for some applications staying constant with the equivalent oxide thickness (EOT)~1.2nm [1]. This lack of scaling of the gate dielectric additionally hinders the targeted scaling of transistor gate length due to higher drain-induced-barrier-lowering (DIBL) and thus higher subthreshold current arising from poorer gate control of channel electrostatics, and/or due to lower carrier mobility from the higher channel doping required to limit the DIBL and subthreshold current for single-gated CMOS designs.

In the prior Research Needs document issued in 2002 for the SRC research cycle that ends this year, the Research Needs for extending CMOS technology up to the 22-nm

1 - Includes input from 8 organizations (AMD, Axcelis, IBM, Intel, Freescale, LSI, SEMATECH, and Texas Instruments)

node included processes and device designs required to overcome these transistor scaling limitations. In particular, the Research Needs included increased efforts in device structures for improved channel electrostatics and technology "boosters" for enhanced channel transport. The channel electrostatics was to be improved by introduction of ultra-shallow, low-resistivity junctions, metal gate electrodes , high-k gate dielectrics, and fully depleted device architectures (including double-gate or triple-gate architectures), while the channel transport was to be enhanced in part by use of materials to increase the mobility of carriers in the channel region. These improvements or "boosters" are now believed to be sufficiently understood and in development throughout the industry [2-7], and are widely expected to be substantially introduced in products before the 22-nm technology node. In some cases, variations of the proposed technology "boosters" are already in production [8,9]. This largely fulfills several high priority items from the previous Research Needs and Gaps document.

The purpose of the present document is to propose an updated R&D strategy and the associated Research Needs related to extending CMOS <u>to and beyond</u> the 22-nm node of the current ITRS roadmap. It is particularly intended to address the Research Needs associated with the front-end aspects of extending CMOS technology. Areas covered include transistor structures, front-end materials, and front-end processes as well as associated characterization. It is noted that a new area of interest is the use of group III–V semiconductors as new channel materials. This is driven by the need to enhance channel transport as well as to reduce power dissipation resulting from lower power-supply voltage, enabled by the use of low bandgap materials. Areas not covered include lithography, device modeling, and back-end processes. Although these are all very important areas that need to be addressed in extending CMOS, they are beyond the scope of the SRC Device Sciences Digital CMOS thrust. However, the impact of device structures and related process technologies on device variation is important and will be considered. Another area also not covered is circuit design and/or circuit techniques to overcome detrimental transistor leakage and power dissipation. It is recognized that the trend of performance doubling every 2-3 years may be limited by power dissipation. While the total power dissipation may be ultimately managed by forced cooling, the

detrimental transistor leakage currents are already forcing circuit designers to adopt power-management techniques such as various sleep-mode design schemes or other bias schemes. These circuit design issues, although very important, will not be addressed in this document, as they are also considered to be outside the scope of the Digital CMOS thrust.

Applications and Roadmap Drivers

Potential application drivers for the roadmap period of interest include personal computers and digital assistants, digital communication products, speech recognition machines and real-time language translators, very-high-resolution video encoders, and petaflop computers. While most of the application drivers listed include various combinations of digital, memory, analog, and RF modules, this document will concentrate on identifying and prioritizing the Research Needs to address the digital technology needs, using as a starting point the technology needs identified by the 2004 ITRS Roadmap.

Scope and Technology Requirements

The scope of this document will be limited to those Research Needs related to extending front-end fabrication of CMOS to and beyond the 22-nm node. This Research Needs document focuses on "CMOS Extension" technologies, i.e., those technologies that, while highly innovative, are still based on the CMOS logic gate as the main building block of digital products. Further, this document covers the Research Needs of front-end processing and materials, and device structures, along with the supporting characterization and metrology techniques. The research needs associated with lithography, back-end processing, modeling, design, and test are beyond the scope of this document.

The technology requirements that historically have been driving CMOS – integration, functional density, speed, and power dissipation - remain unchanged. The major technology barriers to scaling CMOS and improving performance remain - scaling power supply voltage, sustaining low leakage current, increasing drive current, etc. However,

there are qualitative differences between the role various barriers played in the past research periods and the current one as described below. Also, the weight to be placed on filling various gaps is different in the current period.

Current Research Needs & Strategy

The Research Needs of the current research period are organized into five major categories, as shown in Table 1: (1) Device Structures, (2) Gate Stack, (3) Junctions and Contacts, (4) Substrate Engineering, and (5) Characterization and Metrology. All five were included, with slightly different titles, in the 2002 Research Needs document. The Modeling and Simulation category, which appeared in the 2002 edition, has been removed from this edition since it has been addressed by a separate research solicitation.

In comparison to the 2002 edition, this edition of Research Needs has a new and strong focus on new materials and their integration schemes while device architecture is somewhat de-emphasized. The qualitative distinctions between the 2002 edition and this edition, in each of the five categories mentioned above, are described below to emphasize any changes in Research Needs required to extend CMOS to and beyond the 22-nm ITRS node.

1) Device Structure: The 2002 edition included a high priority on development of multiple gate devices. In the past 2-3 years, significant research and development has been focused on multiple gate devices in industry (in addition to the university research); with the improved understanding, these advanced device architectures are now less attractive (i.e. medium priority) as research topics to extend CMOS to and beyond the 22-nm node. The 2002 edition did not include a high priority on process-induced uniaxial channel strain. While it may seem that high priority on such strain should therefore be included in this edition, it is evident that in the past 2-3 years, significant effort has already been put into discovery and development in this area such that several process-induced stressors, including recessed SiGe source/drain or compressive/tensile strained overlayers, have already been implemented as technology "boosters" in high performance 90-nm technology nodes products. The progress in development and understanding of these stressors was so substantial that it is currently perceived as

too mature to warrant high priority for the longer-range scope of this Research Needs document. (It is noted that a medium priority has rather been placed on the scaling limitations of such stressors for planar and non-planar devices.) In this edition, the high priority has instead been assigned towards research on devices with non-silicon high mobility channel materials, in particular, comprised of Group IV or III-V materials.

2) Gate Stack: The 2002 edition included a high priority on many aspects of high-k gate dielectrics including scalability to 1-nm effective inversion gate-oxide thickness, reliability, and effects on carrier mobility; additionally, a high priority was assigned to metal gates with tunable work functions in part compatible with high-k gate dielectrics. Similar to device structures, in the past 2-3 years, significant research and development has been focused on metal gate/high-k gate stacks in industry (in addition to the university research); with the improved understanding, many of the high-priority dielectric topics such as reliability and mobility are now substantially less attractive (i.e. assigned low priority in this edition) as research topics to extend CMOS to and beyond the 22-nm node. In this edition, the high priority has instead been assigned towards research on higher-k gate dielectric materials with further scalability to sub-0.7-nm effective inversion gate-oxide thickness (compared to 1-nm thickness in the prior edition) as well as to research on novel high-k materials compatible with the non-silicon channel materials which were assigned high priority in the Device Structure section of this edition. It is noted that this edition does assign medium priority to research on gate electrodes compatible with these higher-k gate dielectrics to obtain the aggressive effective inversion gate-oxide thickness values.

3) Junctions and Contacts: This edition is very similar to the 2002 edition in that the high priority research needs remain focused on implementation of ultra-shallow, abrupt, low-sheet-resistance junctions and on materials capable of delivering low resistance contacts to source/drain diffusion regions. This is still a critical need for achieving the scaling targets.

4) Substrate Engineering: The 2002 edition included a high priority on development of high-mobility substrates including strained silicon. However, as discussed previously in the Device Structure section, the significant progress on process-induced uniaxial channel strain has resulted in a significant de-emphasis on strained silicon substrates themselves (i.e. assigned low priority in this edition). In this edition, the priority focus has instead been assigned towards research on heterogeneous integration of Group IV or Group III-V high-mobility materials built on silicon (or SOI).

5) Characterization and Metrology: The 2002 edition included high priority on "generic" improvements of electrical and optical characterization of leaky ultra-thin dielectrics, and on high-spatial-resolution strain measurements. Due to the progress on gate stacks with high-k gate dielectrics (see Gate Stack section) with significantly reduced gate leakage, the high priority previously assigned to characterization of leaky dielectrics is now substantially less attractive (i.e. assigned no priority in this edition) as a research topic to extend CMOS to and beyond the 22-nm node. In this edition, the priority focus has shifted from simply leaky dielectric and strain measurements and in fact has become substantially more demanding, requiring physical and/or electrical characterization with high spatial resolution and high precision of stress, gate stack workfunction, defects, doping, etc. Furthermore, this demanding characterization has been extended to three-dimensions as well, with specific focus on non-planar structures, in part due to the significant developments on non-planar multiple-gate device structures in industry as discussed in the Device Structures section.

All five Research Needs categories identified for the current research period are listed in Table 1.

Research Priorities and Funding Gaps

The Research Needs given in Table 1 were ranked in terms of two criteria. First, the Research Needs were prioritized according to their relative importance to extending CMOS to and beyond the 22-nm node. The question asked for this prioritization is "How important is the *knowledge* obtained, related to each Research Need, to extending CMOS

to and beyond the 22-nm node?" This may be referred to as the Research Priority or "Knowledge Gap." Second, the Research Needs were ranked in terms of their funding or "Resource Gap." The question asked for this prioritization is "Given current funding in each research area remains the same, to what extent is each Research Need *adequately funded* to acquire the required knowledge when needed?" The funding includes resources provided by SRC, MARCO, federal agencies, corporate funding, etc. Both of these rankings are quite subjective, but they will guide SRC's solicitation and selection of only those highest quality proposals addressing only those topics most important to extending CMOS to and beyond the 22-nm node.

The importance or Knowledge Gap prioritization by the participating member companies ("Priority" column) was reasonably consistent despite the rather large differences among these member companies in terms of technology infrastructure and CMOS development strategy. The topics were ranked and color-coded into three categories of priority. The result of this ranking is represented in Table 1, where the red, yellow and white colors are assigned to the high, medium, and low priority Research Needs, respectively.

Prioritization of the Research Needs according to their funding or Resource Gaps is also shown in Table 1 ("Gaps" column), where the Research Needs were color-coded into three categories. A Research Need colored in red indicates *substantial additional* per annum funding is needed to acquire the needed knowledge within the required time frame. Yellow means *moderate additional* annual funding is required, and white indicates that the per annum funding for that Research Need is adequate to obtain the needed knowledge in a timely fashion.

References

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8. S. Thompson, et al., “A 90nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1μm^2 SRAM Cell,” IEDM Tech. Digest, pp. 61-64, 2002.

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Legend for Table 1

Priority Legend[1]

High Priority Research Topic	(red)
Medium Priority Research Topic	(yellow)
Low Priority Research Topic	

Funding Gap Legend[2]

Large Funding Gap	(red)
Medium Funding Gap	(yellow)
Small Funding Gap	

[1] There is no relative ranking. All research topics have the same priority within each color group.

[2] A critical assumption in the funding gap ranking is that current funding in these areas remains the same.

Table 1 –Research Needs for Extending CMOS Research Prioritization and Funding Gap Analyses

	Priority	Gap
Device structure		
Ultra-thin-body structures: single gate structures		
Ultra-thin-body structures: multiple gate vertical structures		
Ultra-thin-body structures: multiple gate planar structures		
Group IV high-mobility channel materials integrated with Si		
Group III-V high-mobility channel materials integrated with Si		
Process-induced strain engineering including scaling and limitations for planar and non-planar devices		
Carbon nanotube FETs		
Quasi-1D nanowire FETs		
Gate Stack		
High-k gate dielectrics for planar and non-planar devices capable of 0.7-1.0nm TOXINV		
High-k gate dielectrics for planar and non-planar devices capable of sub-0.7nm TOXINV		
Enhanced carrier mobility for high-k gate stacks & improved understanding of mobility versus TOXINV scaling for high-k/metal gate stacks		
New gate electrode materials for nMOS/pMOS gate work function engineering including multiple-VT devices, for planar and non-planar devices capable of 0.7-1.0nm TOXINV		
New gate electrode materials for nMOS/pMOS gate work function engineering including multiple-VT devices, for planar and non-planar devices capable of sub-0.7nm TOXINV		
Reliability of high-k/metal gate stacks with TOXINV<1nm		
Novel high-k gate dielectrics for non-Si channel materials		
Junctions and Contacts		
Materials development for low-resistance contacts to diffusion including low-Schottky-barrier silicides		
Ultrashallow, abrupt, low-sheet-resistance junctions including study of band-band tunneling, segregation and interface effects in ultrathin Si films and fins		
Low-temperature selective epitaxial growth of Si and SixGe1-x, SixC1-x		
Substrate Engineering		
Group IV high mobility materials heterogeneous integration with Si		
Group III-V high mobility materials heterogeneous integration with Si		
Substrate strain engineering including scaling and limitations for planar and non-planar devices		
New approaches for improved ultra-thin SOI uniformity and roughness for starting substrate thickness < 15nm		
Characterization and Metrology		
High-spatial resolution/high-precision characterization techniques for e.g. stress, workfunction, defectivity, and doping		
3D metrology and characterization with specific focus on non-planar structures		
Characterization of mobility for high-k/metal gate stacks with TOXINV<1nm		
New techniques for measuring workfunction including interface-dipole effects, charge traps, etc.		
Measure EOT or TOXINV or workfunction on unpatterned wafers		