Research Needs for
Memory Technologies

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Requirements and Challenges

Not only memories are intricate part of most integrated circuits, if not all, the popular consumer products in the mass storage space put memory devices as the most common transistors in the market today. Also, flash memory currently serves as the technology driver for most of the critical processing steps. To continue this pace is getting increasingly more challenging, but is important to the whole industry. This document identifies industry-driven research needs for variety of embedded and stand-alone memory devices. It is intended to address novel materials, device concepts, and architectural aspects of memory devices addressing future applications.

This document is also prepared for the purpose of generation and reference of the Call-for-White-Papers in the Device Science Memory Technologies thrust. Within the program structure of GRC-SRC, this thrust only deals with technology-related research. Other memory-related works but focusing on circuit design or compact modeling are included in their respective thrusts, but tied together by the Memory cross-cut.

The general technology requirements are; integration with CMOS, high functional density, high speed, low power dissipation, and low cost. The major technology barriers are stability, reliability, data retention, disturb, and endurance. There is a significant interplay between requirements and barriers, and optimized trade-offs between these are within the scope of this solicitation. The requirements and challenges specific to memory types are listed below [1]:

- DRAM—The one-transistor-one capacitor cell, for both trench and stack capacitors (which are more common), requires etch and photoresist processes of very high aspect ratio. To minimize the capacitor area, high-K dielectrics are a natural path, to follow high-performance logic devices, except for the extra requirement of non-planar surface. To meet retention and refresh requirements, the transistor has to control both subthreshold leakage and junction leakage. Certain novel transistor designs such as those offered by double gates will be useful.

- SRAM— Because this memory is typically constructed from core CMOS devices, all issues associated with MOSFET scaling apply to scaling of SRAM. Additionally, there is a desire to find a dense SRAM replacement that can substantially reduce the area occupied by the traditional 6T SRAM bit cell. Discovery of such a bit cell would have profound implications on the die cost of integrated circuits given the ever-increasing area occupied by this type of memory. In addition to area scaling, there is also a need to develop alternative bit cells that maintain stability while operating at low voltages, thus, allowing the industry to substantially reduce standby power consumption in the memory arrays.
- Nonvolatile Memory: Challenges specific to the device types are listed below. But common to all charge-storing type is the limit of scaling the tunnel oxide while facing the problem of retention for the same required lifetime.
    - Floating-gate type—Pertinent to the floating-gate structures is the requirement for high coupling ratio. This is achieved typically by wrapping around the floating gate by the control gate. Processing for such severe topography gets harder with scaling.
    - Charge-trapping type—The SONOS devices uses a thinner SiN layer to trap charges. They are more planar than the floating-gate type and are easier to scale. Since charges in SiN are not mobile, they can be located either near the source or drain, and such information is counted as 2 bits. The challenges are in general reliability and endurance. Also trapped electron charges are difficult to detrap, and injection of holes needed to neutralize them are more difficult due to higher hole barrier.
    - Non-charge-storage type—This group of newer options require new materials that have not been part of traditional Si processing. Three devices deserve mentioning in this group are FeRAM (e.g., ferroelectric capacitor), MRAM (e.g., magnetic tunnel junction), and PCRAM (phase-change RAM). Multi-level programming on them are generally more difficult.

Research Needs: Categories and Topics

To better identify more specifically the topics of needs for our member companies, we have listed the topics into finer details as shown in the attached table. We organize the Research Needs into three major categories: (1) Embedded Memory, (2) Nonvolatile Memory, and (3) Selection Device. Memory technologies that combine the best aspects of SRAM (speed, ease of integration), DRAM (density), and flash (nonvolatility) are of interest for embedded applications. Within each category we distinguish between material/integration and device/architectural aspects.

Embedded Memory

The desire to integrate large quantities of memory on chip historically has been driven by four main needs: system performance, form factor, power reduction, and memory granularity. In the semiconductor industry today, there are three types of embedded memory beyond the easily-implemented ROM. SRAM is by far the most commonly embedded memory technology and typically dominates die size for many systems. Embedded DRAM has become more attractive if larger quantity of on-chip, volatile memory is required in a given system. The research needs of each are discussed below.

Embedding DRAM into a CMOS process flow has become more popular over the last decade. As a result of the difficulty associated with scaling DRAM technology, there is a need to develop alternative bit cell technologies that can maintain or increase the read/write/refresh performance of embedded DRAM while maintaining the small bit cell area.

Embedding flash nonvolatile memory into CMOS process flows is a common goal in the microcontroller industry. Embedded flash faces different scaling challenges than those found in stand-alone flash technology due to the relatively smaller number of bit cells required. Because of that, the memory array area is dominated by the high-voltage peripheral devices required to write and erase the bit cells (typically +/- 9V). As such, for embedded flash applications, it is critical to find technologies that allow scaling of voltage required to operate the memory array. Development of alternative memory technologies based on resistance changes associated with phase change or based on magnetic tunnel junctions are of interest.

Nonvolatile Memory

The leading nonvolatile memory (NOR flash for code storage and NAND flash for data storage) is facing severe scaling problems stemming from the inability to scale down the tunneling dielectric. We anticipate that research in the following area could extend the life of conventional flash devices: tunneling barrier engineering, new material for storage layers, devices based on asymmetric tunneling, nanocrystal storage elements, devices with multi-bit spatial resolution, devices with distinguishable multiple layers, and 3-D stacking of conventional nonvolatile memory devices in a cost-effective manner.

Research on alternate nonvolatile memory devices (phase-change memory, MRAM, FeRAM) is also part of this solicitation. New materials offer numerous opportunities to develop new nonvolatile memories, which can be used as stand-alone or embedded. Complex metal oxides

and various perovskites can be used for resistive RAM. Ionic conduction or conduction bridges or wires can be exploited in materials like solid electrolytes. MEMS and CNT devices using electromechanical effects can be explored for memory applications. While we acknowledge a breadth of new materials that can be used for memory applications, we emphasize research that combines material research with device characterization. Different architectural solutions that tend to the future product applications are also sought.

Selection Devices

Several new materials and mechanisms are currently being investigated to develop the next-generation memory devices. Most of these approaches rely on non-Si/SiO_2 based memory storage elements and opens up the possibility of stacking several layers of memory arrays on top of the CMOS support circuitry. Much of the literature on these 3D approaches of 2-terminal cells envisages a cross-point memory architecture - each memory storage layer is sandwiched between an array of orthogonal word lines and bit lines. However, an optimally designed addressable/readable memory array implementation without disturbs and with good sense margin requires the insertion of an access device for each memory bit. For a 3D memory, this calls for the ability to fabricate stackable access devices. The attributes required in this device include, aside from the ability to be stacked, adhesion to underlying and overlying layers, low thermal budget for fabrication and dopant activation (within temperatures tolerated by the memory cell materials ~400 C), small geometry, small Ron, low leakage current and, for some applications, bi-directional (bias polarity) operation. It would also result in fewer technology scaling limitations and issues compared to those faced when using a transistor as an access device, where the transistor itself usually becomes the scaling limiter. A thin-film diode fabricated by low-temperature (< 400 C) deposition of polycrystalline or amorphous films could meet the stacking and thermal budget constraints outlined above.

Research Needs: Priorities

Member company representatives were asked to vote on the topics of their preference, with high priority (H) or medium priority (M). Consensus is built on the average of inputs. This methodology yields a total of 6 topics of high priority, and 6 of medium priority, as shown in the table below. It is with these guidelines that we will call for and select proposals in this new cycle of research.

Contributing Memory TAB members:

Tony Pan (TAB Chair)	Applied Materials
Jin Cho	AMD
Ted White	Freescale
Steve Koester	IBM
Sadanand Deshpande	IBM
George Bourianoff	Intel
Greg Atwood	Intel
Mark Stettler	Intel
Scott Summerfeld	TI
Uday Udayakumar	TI
Leonard Rubin	Axcelis
Tsunetoshi Arikado	TEL
Akihisa Sekiguchi	TEL
Mitch Carlson	TEL
Robert Monteverde	TEL
Kwok Ng	SRC

Reference

[1] International Technology Roadmap for Semiconductors (ITRS) 2007 Edition. "*Process Integration, Devices, and Structures*".

Memory Technologies: Topics and Priority

Embedded memory			Priority
SRAM	1a	New memory for SRAM replacement (stability, performance, density, power constraints)	H
	1b	Innovative device/circuit solutions to enable SRAM scaling (stability, performance, density, power constraints)	M
DRAM	1c	New memory for embedded DRAM replacement (stability, retention, performance, density, power constraints)	H
	1d	Innovative device/circuit solutions to enhance DRAM scaling (stability, retention, density, performance, power constraints)	M
Embedded dense memory	1e	New ideas for highly scalable embedded volatile and non-volatile memories addressing issues related to stability, retention, density, performance, power constraints, endurance	H
Novel memories	1f	Embedded MRAM, spin injection MRAM, embedded PCM, and 3-D FRAM	H
Nonvolatile memory			
Device	2a	Scaling of tunneling dielectric (increasing writing and reading speed, improving data retention)	M
	2b	3D memory cell (TFT memory devices, FeRAM capacitors, FinFET)	
	2c	Novel 3D (stacked/integrated) array structures	M
	2d	Nanocrystal memory (single and multilayer, integrated in ONO layers)	M
	2e	Charge trapping/storage layer	
	2f	Multiple bit and multi level storage	
	2g	High-T data retention for flash	
Material	2h	New material for tunneling barrier engineering (blocking layer, storage layer, tunneling dielectric, asymmetric tunneling)	H
	2i	New memory material systems (complex metal oxides, perovskite/correlated oxide memory, solid electrolyte based memory, molecular memory, polymer memory, new material with memory features, and carbon nanotubes with crossbar material)	H
Integration	2j	Integration of memory array based on new material systems (in 2j)	
Selection device			
	3a	Process integration [low-T (<400°C) activation]	M
	3b	Architecture (memory cell dependent addressing, minimizing leakage path in cells)	
	3c	TFT transistors	
	3d	Back-end diode (high current density, reverse breakdown voltage)	