Research Needs for Device Sciences Modeling and Simulation (DSMS), April 2008

Device Sciences
Semiconductor Research Corporation
P.O. Box 12053
Research Triangle Park, NC 27709-2053

Introduction

Technology computer-aided design (TCAD) has become essential to advanced technology development, contributing to solving a diverse range of problems from equipment design and process control through to device compact modeling and design variability analysis. The complexity of a modern technology is such that it could not be successfully completed without extensive use of modeling tools in almost every aspect of its development. At the heart of technology scaling, process and device simulation has played a critical role by giving insight into the relationships between processing choices and device performance that cannot be obtained from physical metrology tools alone. Process and device simulation tools have become a key enabler for the semiconductor industry to continue to achieve increasing device density and performance with high yield and manufacturability.

This document is prepared for the generation of the next call for white papers in the DSMS thrust. Within the program structure of GRC-SRC, TCAD does not include compact modeling which is one of the five thrusts in Device Sciences.

According to the Roadmap, this discipline can be divided into 10 areas. Of particular interest to our thrust, the areas and their descriptions are [1]:

- Front-end process modeling — The simulation of the physical effects of manufacturing steps used to build transistors up to metallization.
- Device modeling — Hierarchy of physically based models for the operational description of active devices.
- Materials modeling — Physical modeling of the properties of materials from atomic to continuum scales to enable process integration and device application.
- Numerical methods — All algorithms needed to implement the models developed in any of the other sections, including grid generations, surface-advancement

techniques, (parallel) solvers for systems of (partial) differential equations, and optimization routines.

The main difficult challenges identified in front-end process for the near term include modeling for SOI and non-planar devices using ultrashort annealing, silicides, and defect formation. Longer-term priorities extend process modeling to beyond-silicon technologies. For device modeling, shorter-term priorities focus on comprehensive 3D silicon device modeling including variability. Longer-term needs include understanding transport and contact properties in beyond-silicon technologies. Challenges are also identified for the Memory and Analog & Mixed-Signal areas. More detailed topics are listed in the table below and are discussed next.

Research Needs: Categories and Topics

The topics in the table are mostly taken from the ITRS Modeling and Simulation chapter as difficult challenges, with some added on by member companies. These topics are divided into three groups: process modeling, device modeling, and general modeling tools. Device modeling also includes electronic properties of materials. Both process and device modeling are sub-divided into short-term (evolutionary) and long-term (revolutionary). Specific topics were added for the Memory and Analog & Mixed-Signal areas to summarize their modeling needs.

Research Needs: Priorities

Member company representatives were asked to vote on the topics of their preference, with high priority (H) or medium priority (M). Consensus was built on the average of inputs. Furthermore, each company was asked to cast a single super-vote on one topic that it feels must be included. This methodology yields a total of 12 topics of high priority, and 11 of medium priority. It is with these guidelines that we will call for and select proposals in this area of research.

1. Process Modeling

1a. Evolutionary CMOS: Doping process physics for conventional and non-classical Si devices

1a.1	SOI structures including partially depleted, fully depleted, ultra-thin body devices, etc. Amorphization and regrowth in Si, s-Si, SiGe, s-SiGe, SOI, including edge effects (i.e. at least 2D); prediction of interdiffusion, residual strain and (point and extended) defects	H
1a.2	Equilibrium and transient diffusion/activation (including interdiffusion, stress effects) in Si, s-Si, SiGe, s-SiGe, SOI including lower temperatures for high-k/metal gate flows, millisecond annealing (Flash, non-melt laser)	H
1a.3	Development of algorithms and numerical methods for accurate and CPU-efficient 3D implant, diffusion, oxidation (moving boundary), stress with interface/strain effects	M
1a.4	Structure and dopant fluctuations, finite size effects	M
1a.5	Pattern, die, and wafer scale uniformity effects in thermal and other processing	M
1a.6	Models for silicide formation including interface effects on contact resistivity	H
1a.7	Defect formation due to stress	H

1b. Evolutionary CMOS: Gate Stack Modeling for 0.5nm EOT and Beyond

1b.1	Prediction of traps, interface states, interface kinetics of high-k materials, including detailed physical modeling of materials and interfaces. Atomistic modeling of workfunction/barrier heights	M
1b.2	Prediction of reliability of high-k/metal gate material stacks	M
1b.3	Impact of dopants on metal gate workfunctions	M

1c. Revolutionary CMOS

1c.1	Diffusion/activation beyond Si (Ge, III-V) – interdiffusion effects, influence of stress, interface properties, implant damage including atomistic modeling connecting structure to electrical properties"	H
1c.2	Modeling of contact formation (germanides, metals, ...)	M

2. Device Modeling

2a. Evolutionary CMOS

2a.1	3D quantum mechanical electrostatics/band structure and physical transport models including strain, high-k/metal gate, UTB, and surface orientation effects	H
2a.2	Novel modeling approaches for device variation effects (LER, RDF, ...) and noise for logic and memory	H
2a.3	Reliability/breakdown physics for high-k/metal gate stacks	M

2b. Revolutionary CMOS

2b.1	Physical models for transport in beyond-Si devices (Ge, III-V) enabling performance prediction/analysis	H
2b.2	Physical models for transport in beyond-Si devices (nanowire, CNT, ...) enabling performance prediction/analysis	M
2b.3	Realistic treatment of transport through contacts (e.g. wire to tube interface in a CNT)	H
2b.4	Efficient simulation of dissipative QM transport, especially using a comprehensive set of scattering mechanisms	H

2c.Memory

2c.1	Modeling novel processes and devices for non-classical memory applications (MRAM, phase change, ferro, nanocrystals, ...)	H

2d. Analog and Mixed-Signal Applications

2d.1	Device/process simulations for active and passive components, physical models for 1/f noise, SOA (safe operating area) and thermal modeling for power devices, novel isolation processes and X-talk, modeling of local parasitic and high frequency behavior of devices	H

3. General Modeling Needs

3.1	Design for manufacturability	M

Contributing DSMS TAB members:

Martin Giles (TAB Chair)	Intel
Mark Foisy (TAB V-Chair)	Freescale
Jin Cho	AMD
Sunderraj Thirupapuliyur	Applied
Michel Frei	Applied
Leonard Rubin	Axcelis
Philip Oldiges	IBM
Steve Furkay	IBM
Mark Stettler	Intel
John Walker	LSI
Jan Kolnik	LSI
Josef Brcka	TEL
Robert Monteverde	TEL
Shaoping Tang	TI
Z Jeff Wu	TI
Ramesh Venugopal	TI
Kwok Ng	SRC

Reference

[1] International Technology Roadmap for Semiconductors (ITRS) 2007 Edition. "Modeling and Simulation".