SRC Research Needs in the Area of Compact Modeling for Design March 2000

Joint Effort of
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Compact Modeling Needs for Design

Compact modeling of transistors has long been a critical step in the IC design cycle. It is becoming ever more important as circuit operating frequencies increase, device tolerances scale down with concomitant increases in chip device count, and analog, RF analog, and digital design styles co-reside on the chip. Thus, SRC design community (in discussions with the Compact Modeling Council (CMC)) is soliciting proposals for compact modeling research in the areas of CMOS and bipolar transistors, as well as black-box modeling, for digital, analog, RF, and RF power applications. Generally, CMOS includes advanced- and natural extensions of bulk CMOS, as well as SOI; and, bipolar includes silicon and HBTs. More details appear in the ensuing documentation.

The scope of this solicitation is limited to "compact modeling" as distinguished from "device modeling". "Compact modeling" refers to the development of models of integrated semiconductor devices where the aim is to reproduce device terminal behavior with accuracy, computational efficiency, ease of parameter extraction, and relative model simplicity for a circuit (like Spice), mixed mode, or system-level simulators. A secondary aim is to provide a computational kernel capable of predictive simulation of terminal characteristics of the N+1 and N+2 technology nodes for digital, analog, and RF devices. The user of the model is the IC designer, and the model interface is considered as part of the model development. Physically based models are often preferred, particularly when concerned with statistical or predictive simulation.

In contrast, "device modeling", usually carried out under the umbrella of TCAD in support of device and process design, is concerned with the understanding and nature of detailed physical representations (often *ab initio*) of device operation, views its audience to be principally device physicists and technologists rather than designers, seeks to be predictive rather than being completely parameterizable from terminal electrical measurements, and does not usually seek computational expediency or model simplicity as its chief goal. With these comments in mind, the following sections outline the aims of this solicitation.

We note that BSIM3, and now BSIM4, has been the *de facto* and recognized CMC industry standard compact model for CMOS for some time. This does not preclude further investigations into CMOS transistor modeling, so long as the goal is marked improvement in the model formulation and accuracy, mathematical treatments, or solution speed. The solicitation committee prefers research efforts that emphasize how the proposed compact models might migrate into mainstream simulation tools.

Please follow the SRC guidelines for submitting your proposal. These guidelines are shown at http://www.src.org/univ/proprep/proposal.dgw. Each of the requested topics is enumerated. In your proposal, YOU MUST SPECIFY THE IDENTIFICATION NUMBERS OF THE TOPICS TO WHICH YOU ARE RESPONDING, as this facilitates our distribution of the proposals to the reviewers. For example, one could identify work on gate tunneling current (1.1.1.1) for SOI MOSFETS (1.1.2.1).

Following is the timetable for this solicitation:

Table 1: Schedule for compact modeling solicitation

Date	Milestone Activity
March 29	Post solicitation on SRC Web Site
April 28	Proposals due to SRC
June 9	Notification of contract awards
June 27	Kick off meeting at TCAD review, location TBA
July 1	Funding starts

The SRC expects to fund 3-5 research tasks for a three-year period. Normally, the granularity of SRC contract funding is in 1-2 graduate students, including university overhead and faculty time.

The rank-ordered list of SRC interests in compact modeling for this RFP are as follows. More detail appears in the discussion below.

(1) MOSFETs
(2) bipolar transistors
(3) "black-box", empirically-based models that enable the investigation of devices that may not yet justify a full effort to develop physically-based compact models.

1.0 MOSFETs

SRC plans to fund dual projects in the CMOS compact modeling arena: (1) extensions to BSIM to assure its continued viability as the industry standard model, and (2) proposals for new CMOS compact models, particularly those with novel depictions of underlying physical mechanisms (such as, but not limited to, the charge-sheet model) that may themselves eventually become industry standards.

As item (1) suggests, industry's adoption of BSIM has resulted in a substantial BSIM-oriented infrastructure (*i.e.*, extraction methods, device structures, experience, *etc.*). It has also become the standard interface between design and technology groups, both for intra-company groups and design-foundry partnerships. Because many in the industry depend on BSIM, SRC invites proposals that aim to extend BSIM's capabilities, adhering to the principle of physical integrity wherever possible.

Referring to item (2) above, the industrial community is actively debating the merits of present CMOS compact modeling approaches (including BSIM) as devices scale below the 70nm regime. Most believe that a single, physically-based model kernel could likely be the common foundation for the disparate demands of CMOS, provided that the correct model extensions emerge for analog, RF, and scaled digital transistors, whether those devices appear in deep-submicron bulk or SOI technologies. A common kernel would be desirable since it would facilitate uniformity in model implementation and functionality in the host simulator, as well as in parameter extraction. Therefore, the proposed investigator is encouraged to consider a migration path of any proposed model from concept to full integration as a standard device model. In particular, use of a standard interface, such as Verilog-A, is one desirable means for technology insertion. Responders to this RFP should describe how they intend to handle the issue of making models available.

It is important that the proposal clearly explains the merits of the offered modeling approach and specifically addresses how it improves upon the existing state of the art.

1.1 MOSFET Modeling Needs

Section 1.1.1 lists the set of MOSFET model features identified as areas in need of research. These define a model core or kernel that could be used for simulation of bulk MOSFETs and with appropriate extensions simulations of the transistor types listed in Section 1.1.2.

1.1.1 Core MOSFET Model Features (with general prioritization of interest)

- 1.1.1.1 gate tunneling current
- 1.1.1.2 gate-induced drain leakage (GIDL)
- 1.1.1.3 hot electron current
- 1.1.1.4 output impedance model that includes the effects of (possibly asymmetric) pocket implants, velocity overshoot, and accurately represents the transition from linear to saturation region
- 1.1.1.5 asymmetric MOSFETs, esp. source and drain resistivity and capacitances, asymmetric pockets and halos
- 1.1.1.6 graded lateral channels

1.1.1.7 accommodation of hi-K gates

1.1.1.8 high-speed/RF modeling that includes layout-dependent RF substrate resistance and capacitance models that provide a good balance between efficiency and accuracy

1.1.1.9 meaningful model parameters that facilitate parameter extraction

1.1.1.10 comprehension of the physical factors driving process variation in device parameters, particular gds. This is more often treated by principal component analysis which models a particular manufacturing line at a particular time but does not provide physical understanding.

1.1.1.11 MOSFET noise, including dependence on hot-carrier effects. Also, improvement in 1/f, thermal, as well as other noise sources.

1.1.1.12 non-quasistatic effects

1.1.1.13 accommodation of CMOS RF power devices that reside on CMOS chips will need a model which can be extended to include drift regions, which are similar to 3-terminal resistors, and accumulation regions.

1.1.1.14 capability of handling the 'new' devices that result from scaling below 70nm and from integrating more diverse MOSFET devices on-chip and directly in a system.

1.1.1.15 an extraction method for L-effective of bulk and SOI MOSFETs that is accurate for sub .1 micron devices and is able to deal with variations in print bias with design length

1.1.1.16 self-heating effects

1.1.1.17 temperature modeling

1.1.1.18 SOI model that accurately predicts source-drain breakdown based on accurate high current models for the bipolar, FET and impact ionization.

1.1.1.19 multiple V_T support. If it turns out that more than an empirical model is required to achieve this item, then it should be prioritized higher. In that case, SRC would consider proposals for a physically-based model (unpinned surface potential, comprehends vertical and lateral non-uniform doping in a self-consistent manner, etc.). If you respond to this item, please discuss your rationale for selecting either "empirical" or "more physical".

1.1.2 Extensions of Core Model Defined in 1.1.1

1.1.2.1 Bulk MOSFETs for sub-100nm

1.1.2.2 SOI MOSFETs

1.1.2.3 power transistors, i.e., LDMOS and DEMOS, including RF transistors

1.1.2.4 FAMOS transistors, including coupling effects of the floating gate

1.1.2.5 nonplanar device structures, such as those being developed in sub-100nm regime

2.0 Bipolar

Research is needed in the area of modeling advanced silicon and SiGe BJTs for high-speed/RF circuit applications, including non-quasistatic effects, and heterojunction barrier effects. Compatibility with existing models (Gummel-Poon, Kull *et al*., or VBIC) may be a plus in terms of model insertion; however, SRC will consider other model approaches. Submitters must explain the expected benefits of their model approaches.

3.0 Novel "compact modeling" schemes, particularly for nonconventional devices

Accurate, very fast models: This requires a new look at fast models that are extracted from other models and/or measurement data. The predecessor would be the David Root table look-up model, but table look-up itself is not required or necessarily desired. A company can implement or use an accurate model in a circuit simulator that is just too slow or has too many discontinuities to effectively enable a circuit simulation. A fast, data-compressed 'table look-up' model is required that would be quickly extracted from a compact model and then run very quickly, robustly, and accurately.

This model should also be extractable from sets of measurement data (DC, CV, s-parameter, memory-effects (thermal, trapping)) and be verifiable against RF FOM such as IP3 and guarantee consistency between small- and large-signal models. The model should be multi-noded, easily handle at least 5 nodes and be technology independent. Also, the model provide for generalized scaling of 3 or more parameters.

First application of this model could be for HEMTs and RF power devices, but it should be extendable to non-bulk CMOS, QCA's, quantum dots and any other electrical component.