# Research Needs for Circuit Design

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Emphasis on circuit design research is essential if SRC member companies are to reap the chip performance advances predicted by the ITRS.  This is especially true in the present environment of deep submicron technology scaling where the confluence of daunting physical limitations – high transistor leakage currents, more resistive interconnections, significant electromagnetic signal coupling, increasing 1/f and thermal noise due to hot electron effects, reduced signal swing due to voltage scaling, higher current requirements to reduce thermal noise, and the like – threatens to impede the pace of future performance gains.

Circuit design research is a continuing interest of the SRC member companies due to their growing concern over design challenges facing them in the future and due to an expected shortage of graduating engineers skilled in the design discipline.  Thus, the intent of this report is to help stimulate the imagination and creativity of the academic circuits research community by presenting a contemporary view of circuits needs and challenges as viewed by industry.  Specific challenge problems listed in each section below are prototypical and are intended to illustrate complexity level as well as capture critical areas of need from the member companies; however, it is not intended that the numerical goals be narrowly targeted. Interested investigators should focus on research results that are germane to the 3-7 year time horizons. The problems in the following sections are listed in approximate priority order.

The ICSS committee encourages researchers to address process issues that are related to decreasing device size including leakage effects. ICSS will de-prioritize proposals that use outdated process files. In order to facilitate usage of a baseline process file for all circuit design researchers to use, ICSS has funded Professor Chenming Hu on a project titled "**Benchmarking Year 2003-2006 Circuits Today**". This project is tasked to create predictive SPICE model files for 100 nm, 70nm, and 50 nm processes which have the flexibility to consider a wide variety of anticipated issues associated with decreasing features sizes of devices. More information and actual model files may be found at http://www-device.eecs.berkeley.edu/~ptm. Other researchers are welcome to suggest alternative SPICE model files as well that comprehend issues associated with VDSM scaling issues. Please send the URL to Justin Harlow(harlow@src.org) to have the link placed on the SRC website for other researchers to reference.

# 1.    Process and Circuit Interface

## 1.1    *Barriers:*

The increasing cost and complexity of maintaining drive current densities (A/µm of width) under constant field scaling is a <u>fundamental barrier</u> to maintaining the customary performance increases (~30%  improvement per generation in per-stage delay).  It seems increasingly likely that aggressive oxide scaling alone will not provide the performance gains desired by industry.  Companies must rely on innovative circuit design techniques as a complement to device technology scaling to realize continued performance gains. Design will also need to accommodate non-ideal device properties, e.g., high-leakage-current transistors, large wiring delay relative to gate delay, low signal swing, and the like.

As integrated circuit products have been pushed to ever higher levels of integration and performance, the impacts of uncertainty have grown and existing design methods have become increasingly poor at managing these impacts. As a result, alternative approaches to managing the risks posed by variation need to be adopted. This means that uncertainty needs to be considered more explicitly and more rigorously in more areas of design. To this end, research should address the following issues associated with variation in digital design.

(a) Accurate models of the spatial and temporal variations in device and interconnect parameters in modern manufacturing technologies (sub-0.1 micron)
(b) Accurate and computationally efficient techniques for predicting the impacts of these variations on large circuits (e.g., clock trees, adders, PLL's)
(c) Accurate techniques for incorporating these variations into timing analysis
(d) Accurate and computationally-efficient techniques for optimizing circuits, balancing the impacts of variation with performance, power, area, noise, etc.
(e) Families of circuits resistant to these variations

## 1.2    *Research Vectors:*

Research focusing on the circuit implications of <100 nm ($L_{eff}$) devices.  In particular:

(a) Circuits that comprehend, manage and possibly leverage the effects of large subthreshold source-drain leakage currents (in the hundreds of nA/µm) due to process scaling, high operating temperatures, etc.

(b) Circuits that do the same for the effects of large gate leakage currents (in the tens of nA or more)

(c) Circuits that exploit the RF potential for aggressively scaled digital CMOS.  What process/circuit innovations will enable efficient, dual operation of both RF and rail-to-rail circuits?

(d) Circuit and process interactions that will permit continued aggressive voltage scaling in the face of <u>decreasing</u> saturation currents. Innovative solutions that <u>decrease dependence on process scaling</u> as a vehicle for performance improvement. We seek ideas to accommodate increasing process tolerance, with low performance penalty, through circuit techniques.

(e) Low-cost circuit and process techniques for improving soft-error immunity in sub-100 nm Leff technology generation.

(f) Viable SOI circuit family alternatives. Do they exist? What are they? This research must comprehend anticipated improvements in cost/performance of bulk CMOS.

(g) Novel device structures that permit complex circuit operations at the device level. This research could leverage the state of the art in EEPROM technology

(h) Research that rethinks fundamental concepts of S/N ratios from the device upwards and targets solutions for micro/millivolt signal swings for digital systems.

(i) Adaptive, self-compensating circuits to combat local device and interconnect variations, especially as relates to clock skew, and local variations in clock loading.

(j) Methods that leverage off existing devices and technologies in the design (such as DRAM trenches) for implementing large, on-chip decoupling capacitance, and design methodologies which distribute the expensive decoupling capacitance resource optimally.

(k) Methods of designing , modeling and measuring ESD protection devices with low capacitance and resistance for the very sensitive process of 2007. This could involve package designs with built-in protection networks.

(l) Circuit architectural methods which address a strongly Electro-Migration limited metalization.

(m) Analog circuits that exploit the bipolar nature of leaky CMOS technology; for cost effective, highly integrated systems.

(n) Circuits that handle the increasing statistical variability of smaller numbers of dopant atoms and patterning at the diffraction limits of light. We solicit ideas that quantify and subsequently correct for these effects with minimal performance penalty. Circuit families of special interest include: cache cells, data path latches, sense amplifiers, and self-calibrating analog circuits.

### 1.3    *Challenge problems:*

**1.3.1**  Develop logic families for the <70 nm technology generation that assume a <u>reduction in Idsat from previous generations</u>, no scaling of oxide thickness, Vt variations

of ~25% and operate in the sub-1V regime. The research could include novel device structures in addition to circuit topologies. These logic families should address the issues of noise immunity, speed, and power consumption.

**1.3.2** Develop low-cost process/circuit enhancements for realizing analog elements with a per-stage gain of >40dB at a GBW of 20 GHz, $10nV/\sqrt{Hz}$ noise on a 150 Ghz $f_T$ process ($L_{eff}$ 70-100nm). This research could use regimes of sub-micron CMOS that are uninteresting for digital circuits and possibly multiple voltages. Ideas in Vt control, leakage control, low voltage gain enhancement as well as improvements in circuit/layout techniques to reduce circuit-induced noise affecting critical nodes are especially welcome.

# 2. Large scale digital circuits (ASIC and full custom)

## 2.1 *Barriers:*

Power delivery, noise immunity, reliable clocking and power dissipation are key limiters to continued performance/density improvements. It seems appropriate to revisit the assumptions underlying voltage scaling, since the charge demand from the power delivery system is cause for concern.

## 2.2 Research Vectors:

(a) Circuit research that is closely coupled to architectural innovations for developing low power scaleable digital systems such as a circuit design which lends itself to overall lower power at the architectural level.

(b) Innovative memory hierarchy proposals including the use of embedded DRAM plus high performance logic and improved SRAMs (performance and density) are needed to deal with the ever widening gap between memory and processor performance.

(c) Circuit level advances that reduce the cost/complexity of design for test. Approaches to $I_{ddq}$ style testing in leaky domains.

(d) Low voltage, power electronics research in deep submicron processes. In contrast to the current situation where advances in power converters occur primarily at technology that is two or more generations behind, we solicit innovative ideas for DC-DC converter designs and/or adaptive system design that exploits the high current and low voltage capability of 100nm or less CMOS devices.

(e) Alternatives to aggressive voltage scaling as the way to breach the power wall that all SRC Member Companies face. Possibilities include noise tolerant, ultra-low-swing schemes and further research in scaleable dynamic circuits as well as novel adiabatic-style circuits that comprehend advances in process/on-chip magnetics. (Caution: a lot of work done in this area. New ideas should lead to and support large-scale manufacturable solutions).

(f) New approaches to synchronous systems that reduce requirements on clock skew/jitter and on power delivery. This could include multiple clock domains, incorporation of mesochronous systems (one clock frequency with phase differences

between communicating circuitry due to skew), plesiochronous systems (several clock sources of the same frequency within a Crystal tolerance), as well as approaches to asynchronous systems. We strongly urge that proposals in this area comprehend the design tool flow and large scale testability of any innovations.

(g) Circuit architecture research that comprehends inductive effects in lossy interconnects and power distribution networks. We recommend that proposals also address the increasing dependence of system performance on interconnect scaling. Circuit techniques that intelligently leverage coupling (electrostatic and magnetic) and/or ameliorate this trend are especially welcome.

(h) Development of standard at-speed test circuits that are either on-chip (BIST) or on-wafer (BOST) which challenge device and interconnect limitations and enable faster feedback on performance. Examples of this would be on-chip evaluations for noise, crosstalk, delay jitter, etc., or off-chip testing for timings, noise, etc. For BIST, this would include suitable stimulus circuits that replicate digital system activity at the local and (possibly) semi-global level.

(i) Innovative methods of reshaping state-of-the-art front-end analog processing for improving the robustness of subsequent digital processing. We solicit proposals that could include frequency domain techniques for performance enhancement (e.g. FFT).

(j) Circuit techniques that comprehend upgradability. We solicit on-chip circuit ideas that incorporate flexibility and dynamic upgradability (*e.g.*, reconfigurable fault tolerance).

(k) Develop memory architectures with integrated per bit processing, eg. Content Addressable Memories. Processing the data in the memory (as opposed to accessing and sending to a centrally located device and then re-storing) should alleviate some of the interconnect communication problems.

(l) Explore novel chip-based techniques of reducing Electro-Magnetic Interference. Develop methodologies for identifying where EMI is a problem and how to avoid it at the circuit design level.

(m) Novel circuit techniques that exploit low-temperature operation. This research can be multi-disciplinary to include low-cost system level cooling options and device optimization for low temperature operation as well. The purpose is to address the possibility of temperature scaling for increasing performance as opposed to process scaling.

(n) Novel signaling for low cost, low power, high bandwith chip-to-chip communication that relieves  pin count constraints. This could include multi-level signaling, high speed serial with equalization, optical interconnect. Proposals should address feasibility of high volume manufacturing.

**2.3** *Challenge problems:*

**2.3.1** Develop 10 GHz, low-power data path circuits for processes beyond 100 nm. These circuits (adders, multipliers, barrel shifters) should incorporate novel intra-die data transferring schemes, and work in aggressively voltage scaled regimes (400-600mV Vcc)

**2.3.2** Develop <u>noise tolerant</u> circuit design techniques. Multidisciplinary research that comprehends the aggressor (device/circuit), transmission medium (interconnect), and victim (device/circuit). We expect robust circuits that perform reliably at 10-20ps edge rates with 100nm wide interconnects(i.e., narrowest drawable line) and device Vt of 100-300mV. We seek proposals that <u>rethink traditional tradeoffs between noise immunity and performance</u> in digital systems. In particular, we welcome initiatives that approach circuit design with probabilistic benchmarks in mind, so that more radical noise immunity proposals can be entertained.

**2.3.3** Deliver power efficiently at 300-500mV, 100-200A for highly integrated systems on a chip. Multidisciplinary research that comprehends low cost packages, on/off chip decoupling, novel circuit techniques for power conversion and power grid design. Additional collateral in understanding the nature of power grid noise for enabling large scale integration. We strongly encourage interaction with research in the process area relevant to on-chip magnetics.

**2.3.4** Develop clock delivery mechanisms at 10 GHz with <5ps of jitter. The research should comprehend novel PLL/DLL schemes, other mixed signal adaptive methods and layout techniques. Awareness of advances in interconnects and packages is required. Again, we welcome multidisciplinary proposals in conjunction with experts from testing and packaging

**2.3.5** Do a large-scale, simulated design using the projected characteristics of 2007 process. For example, get a SPICE model for a 70 nm gate transistor with high-k dielectric, asymmetrical channel, high sub-threshold and gate leakage in an SOI process. Project the technology file for a 100 nm design rule interconnect system with high resistance and coupling and use this for parasitic extraction. Assume clock frequencies of 10 GHz. Consider power dissipation of utmost importance. Novel ways of getting data throughput and maintaining clock frequency while maximizing the logical operations between registers is desired.. Across-chip line width variation (10nm for a 70 nm poly width) will limit circuit flexibility.

# 3. Core Analog/RF elements

## 3.1 *Barriers:*

Aggressive voltage scaling is a mixed blessing, at best, for core analog elements. Novel techniques will have to be developed for the leaky low voltage regime. Since velocity saturation occurs at lower drain voltages , the transconductance per unit current ($g_m/I_{dsat}$) will be low. However, this may be partly offset by increased $I_{dsat}$ per unit area and improving $f_T$. In addition, it should be emphasized that reduced supply voltages will directly impact achievable dynamic range and that for inductively loaded networks where signal excursions can exceed the supply voltage, breakdown or impact ionization effects

may limit performance. Also, techniques must be developed that provide maximum supply noise rejection. Analog techniques should make minimal additional demands on increasingly expensive process technologies.

## 3.2    *Research Vectors:*

(a) Continued research in CMOS RF (1-10GHz) building blocks including LNA's, image rejection mixers, balanced quadrature up/down converters. New approaches/techniques are encouraged as well as continual evolutionary improvements as technology permits.  Push the limits of performance with respect to frequency band, noise figure, linearity, and intermodulation suppression. Investigate methods to achieve low cost, high Q (>200)  passive elements which may include simple process enhancements such as ferrite films or MEM approaches which demand simple process enhancements.

(b) Improved building blocks including OTA's, opamps, ultra-linear transconductors, voltage/current references, etc. with an emphasis on low power approaches. Consider approaches compatible with SIA roadmaps in 3-7 years for CMOS and BiCMOS (SiGe). New techniques using current mode or log domain approaches should be considered.

(c) Develop new power amp techniques with characteristics of high linearity/high efficiency having a low power output (100 mW to 200 mW range). Concentrate on BiCMOS/CMOS and SiGe technology.

(d) Develop methods for on chip T/R switches with high Zoff/Zon ratio and good isolation. This may come in the form of new architectural methods or new component approaches as simple process add-ons.

(e) As frequencies increase, package/PCB effects will not be able to be separately considered from the IC circuit design (5-20GHz). Methods to include the package and PCB in the intrinsic design must be developed and exploited. Package/PCB design will most likely be performed concurrently and both engineering teams will need to have an understanding of the cross-disciplinary issues. Research into new circuit techniques that consider parasitic and transmission line effects are encouraged.

(f) Investigate novel broadband techniques for RF applications in the 1-3GHz range (for example those that use resistive feedback or low Q inductance techniques as opposed to inductive narrowband approaches). Exploit new process speed/performance advantages. Determine limitations and suggest optimal applications.

## 3.3    *Challenge problems:*

**3.3.1** Develop integrated CMOS receiver/transmitter pairs and timing circuits for 10-20GB/s per pin data transmission circuits. This research should be fully cognizant of board/cable interconnect technology. The circuits should support heterogeneous

voltage supply (600mV through 1.2V or two technology generations).  A typical power constraint  is <5mW per pin.

**3.3.2** A fully integrated "low phase noise (<-125 dBc/Hz) RF VCO" in $\leq 0.18$ μm CMOS process.

**3.3.3** Develop capability to enable 'retargetability' of general or specific analog/mixed signal IP blocks. The objective is to allow for rapid migration to next generation technologies and represents both a design and CAD challenge

## 4.    Mixed signal/systems on a chip

### 4.1    *Barriers:*

Continued integration of analog and digital components is a fundamental precept of all SRC Member Companies.  Management of noise (substrate-coupled and otherwise) is likely to remain the fundamental barrier.  At $L_{eff}$ < 0.25μm, 5GHz radio front ends in CMOS will become a reality.  The potential for simultaneous on-chip digital processing at  these speeds is enormous.  <u>The challenge is to achieve the high performance possible with these technologies in a low cost, integrated package.</u>  In the case of communication systems the goal is the elimination of expensive precision off-chip components.  For sensors and DSP systems, low power, enhanced S/N ratios and small die sizes remain key.

In addition to design related issues, test and evaluation of complex mixed-signal devices will become ever more difficult.  Since functions will be embedded, they may not be observable. New test paradigms or DFT are necessary as applied to mixed-signal.

### 4.2    *Research Vectors:*

(a) Breakthroughs in data converter design resolution and power that will enable new applications such as software radio, optical equalization etc.

(b) New monolithic VCO techniques from 1 – 10 GHz that are quadrature capable. Emphasis should be on low power, low voltage, and very low phase noise.

(c) New digital circuit approaches that are inherently lower noise. Quantify size and power implications. New interface approaches that minimize coupling to sensitive analog networks (current mode for example).

(d) Circuit and possibly process solutions that rethink the state of the art for reducing and tolerating substrate coupling.  Measurement based comparisons of competing noise tolerant schemes and characterization of achievable analog performance in a given process.  We encourage ideas that reduce the signal communication between noisy and quiet sections of mixed signal systems.  We urge that proposals focus on circuit/measurement rather than CAD oriented characterizations.

(e) Since the capability for analog and digital exists, research methods that exploit the power of DSP to enhance analog circuit performance through feedback or calibration. Research circuit techniques as well as observability and measurement approaches to derive feedback or calibration signals. Extend beyond data converters to other analog functions.

(f) Research new test methods for complex systems on chip. Consider new paradigms in procedure to "design for test" or develop approaches for Built In Self Test for analog/mixed signal and RF.

(g) Communications networking circuits which are low cost with high bandwidth. We strongly urge that circuit developments provide low cost solutions for optimizing bandwidth usage on other band-limited media.

## 4.3    *Challenge Problems:*

**4.3.1**   A 16 bit CMOS A/D converter for a digital radio receiver.  Nyquist rate conversion conversion at 20MHz with IF at 10MHz.  Differential and integral non-linearity at ½ LSB levels and a 96dB spur free dynamic range.  This will  require a sample and hold with jitter low enough to sample a 10MHz signal with errors below 99dB relative to the reference. Phase noise requirement in this problem is about 10x better than what can currently be produced by a crystal oscillator timing reference. The solution in this problem will require enormous improvement in timing references in addition to an A/D circuit design.

**4.3.2**   A low cost direct conversion (RF-baseband) GSM receiver in CMOS. GSM/DCS1800 standards for 900/1800 MHz systems.  Channel bandwidth 200KHz, sensitivity S/N = −110 dBM, at <40mW power.

**4.3.3**   Sigma-delta type oversampling data converters operating with GHz clock CMOS in 0.18 μm or smaller feature size, standard digital CMOS processes.

**4.3.4**   Driver circuit operating with a power supply of 2.5V and having to drive 5V peak-to-peak at 200 MHz in 0.35 μm process.  This is an example of a class of high frequency driver circuits that will be required to support heterogeneous voltages.

**4.3.5**   Explore passive and active silicon-based optoelectronic circuits. It is essential to leverage the silicon manufacturing expertise, possibly including silicon-on-insulator. Passive circuits include (but are not limited to) waveguides, multi-mode interference couplers, directional couplers, DWDM waveguide gratings. In the area of active optoelectronic circuits: explore optical computing structures. Integration of silicon structures with III-V devices can also be addressed, but only to enable the main research goals (active and passive circuits described above).