Semiconductor Research Corporation

Research Needs for Integrated System Design
Integrated Circuits and Systems Sciences
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1. Purpose

This document is a significant update from the 2000 ICSS "Research Needs for Integrated Systems Design" document and is a joint effort by industry experts in the systems design discipline. The purpose of this document is to provide university researchers interested in this area a set of industry needs looking forward five to ten years, and to encourage university research in these areas.

2. Scope

The nature of integrated systems is changing dramatically and rapidly. In the 1990s, the personal computer drove progress in microprocessors, memory, and local area networking. In the 2000s, the dominant high volume, consumer level system will be portable, wireless derivatives of today's digital cell phones and Personal Digital Assistants (PDAs). These devices will have dedicated IP addresses and will be constantly linked to the worldwide Internet. They will largely replace today's personal computers and telephones as the primary portal for the user's communications, navigation, mail, banking, and learning. They will link to stationary devices for large area data and multimedia display, but will be intensely personal tools. They will incorporate speech recognition and synthesis, as well as live two-way video in the later years of the decade.

The new breed of systems outlined above will necessitate research on many fronts. In particular, there are major challenges in system architecture exploration, modeling, and synthesis. Multimedia processor design, which will consist largely of mixed signal and digital signal processing subsystems will dominate advanced system design and will require new tools and methodologies. A high degree of reconfigurability and adaptability will be required in advanced systems, in order to rapidly adapt to developments in communications protocols and respond to shrinking product life cycles. Power management and conservation will be of supreme importance in all designs. Built-in RF communications circuitry will be ubiquitous.

The supporting fabrication technologies will continue to play a key role in the realization of systems. Continued shrinking of devices and interconnect systems will require increasingly accurate design-level models, which capture not only performance, but statistical variations. System design, beginning with the most abstract architectural exploration phases and continuing to physical implementation, must comprehend the opportunities and limitations of advancing device, interconnection, and packaging technologies.

New integrated system designs are needed that will allow increased levels of integration and heterogeneity (*e.g.* mixed-signal, sensors, MEMS, passives, etc.), increased software programmability/configurability, and improved design speed and flexibility. The research needs outlined in this document are arbitrarily organized into the categories of Applications, Algorithms, and Architectures. This classification is used for convenience, and is not intended to limit the span or scope of proposed research. Proposals that encompass activity in any or all of these categories, or in related categories that are not explicitly stated, are welcome (researchers please refer to http://www.src.org/research/rfpsearch.dgw for current funding opportunities).

3. Application Focused Research Topics

3.1. High Bandwidth Communications
3.1.1. High speed sorting and routing of data to diverse applications
3.1.2. High speed, high volume, multiple key searches of large data bases
3.1.3. High speed, highly secure encryption/decryption techniques and architectures
3.1.4. Improved, and Novel, RTOS architectures that support high levels of concurrent applications
3.1.5. Improved and Novel physical layer architectures to support high speed links
3.1.6. Channel equalization methods: Adaptive, Continuous time, and discrete time FIRs, etc.

3.2. Wireless communications
3.2.1. Novel, efficient modulation and demodulation schemes
3.2.2. Novel applications of current technologies like TDMA, FDMA, and CDMA spread spectrum techniques
3.2.3. Techniques to optimize co-existence of spectrally close channels
3.2.4. Ultra Wide Band communication schemes

3.3. Personal Communications
3.3.1. Ultra low power RF links
3.3.2. Always on communication links – dynamic adaptation to optimal channel available
3.3.3. Power and form-factor optimized architectures to support real time audio-video communications: Processors, displays, transducers, batteries, and radios.
3.3.4. Highly secure communications – personal (bio-metric?) authentication and encryption techniques

3.4. High performance Audio and Video stream processing
3.4.1. High performance processors to encode and decode data streams
3.4.2. Novel logic level building blocks for communications processors
3.4.3. Novel techniques to synthesize communications (DSP) processors from high level descriptions.
3.4.4. Rapidly filed programmable communications processors to accommodate dynamically changing protocol and application needs.

4. Algorithms

4.1. Abstract models of computation and specification that can be used to efficiently implement both small and large systems.

4.2. Novel algorithms and data representations to efficiently implement:
4.2.1. High-performance computing systems
4.2.2. Reactive control systems
4.2.3. Data flow solutions

4.3. Novel algorithms or restructured algorithms to:
4.3.1. Reduce power consumption.
4.3.2. Allow tradeoffs between power consumption and performance.
4.3.3. Enable or enhance fault tolerance and/or reliability.

4.4. Novel algorithms (such as video or audio compression and decompression) that are executed efficiently on existing or novel IC architectures.

4.5. Algorithms to enhance application performance when executed on emerging new architectures.

4.6. System design techniques to evaluate the statistical distribution of computing requirements (such as computation MIPS or communication bandwidth) of multitasking systems. These should evaluate average, worst and best case requirements.

4.7. Algorithms to prune the total number of potential architectural solutions.

4.8. Efficient algorithms and tools for design partitioning and hierarchy.

4.9. Tools for efficient direct compilation (with optimization) of algorithms and high-level models into hardware. Ensure mathematical correctness of the translation.

4.10. Algorithms to determine the optimum amount of memory (registers, cache memory, main memory and mass storage) for applications, such as efficient execution and cost-effective implementation of a selected video processing algorithm.

4.11. Techniques to measure design and algorithm quality

    4.11.1. Assess designs resulting from EDA tools.

    4.11.2. Evaluate the quality of algorithms with respect to eventual implementation.

    4.11.3. Compare alternative designs or alternative algorithms with respect to complexity, performance, power or other critical measures.

    4.11.4. Develop efficient alternative mathematical techniques for existing algorithms.

5. Architectures

5.1. New system architectures that are deep-submicron-aware, accounting for noise, power, timing, interconnects, etc.

    5.1.1. SoC designs that support low-cost verification and test

    5.1.2. Reliability issues in noisy environments

    5.1.3. Cost and battery-life constraints in mobile appliances

    5.1.4. Communication efficiency, bus bandwidths and signal/pin count constraints in future design

    5.1.5. Interfacing and integration issues in mixed electro-optical Interconnect architectures

    5.1.6. Architectural support for self-calibration of system analog blocks

5.2. Novel system architectures enabled by inclusion of non-traditional technologies

    5.2.1. Optics and the use of III-V compounds such as InP and GaAs

    5.2.2. Magnetic materials and structures

    5.2.3. Embedded microstructures and microsystems: mechanical, electrical and electro-mechanical (e.g. MEMS)

    5.2.4. RF and microwaves

    5.2.5. Organic compounds and materials

    5.2.6. Other non-silicon based technologies

5.3. Efficient architectural support for algorithms to process integrated applications:

    5.3.1. Real-time audio (speech and music)

    5.3.2. Video (real-time camera and music)

    5.3.3. Data (application data, internet)

5.4. Microarchitecture research including:

    5.4.1. Instruction-level and/or fine grain parallelism

    5.4.2. Complexity-, power- and verification-efficient microarchitectures

    5.4.3. Advances in: superscalar, VLIW, SIMD/Vector, multiscalar, multithreaded, chip multiprocessors (CMP), etc.

    5.4.4. Adaptive or polymorphous processors: those that support application-driven resizing and reconfiguration.

    5.4.5. Asynchronous, self-timed and multiple-clock processing, with design tool support

    5.4.6. Other advanced processor paradigms (including memory hierarchy support) aimed at high performance at low power.

5.5. Novel hardware/software interface architectures

5.6. Special-purpose, or programmable microarchitectures to support emerging new applications:

    5.6.1.1. Multimedia, DSP processing specific to game software

    5.6.1.2. Cryptographic applications (related to internet security and privacy)

    5.6.1.3. New generation graphics, image and signal processing

5.7. Techniques for (cycle-accurate) performance and power-performance modeling of:

    5.7.1. Pipelined, advanced superscalar microprocessors; with optional SIMD acceleration hardware

    5.7.2. Chip multiprocessors and multithreaded processors

    5.7.3. Synchronous designs with embedded asynchronous blocks

    5.7.4. Workload characterization and trace generation issues in systems modeling

5.8. Abstract or high-level modeling to support early-stage design space exploration

    5.8.1. Bounds models and other analytical modeling techniques

    5.8.2. Hybrid (analytical-simulation) models

    5.8.3. Statistical modeling

5.9. Evaluation and Measurement of Architectural Paradigms

5.9.1. Estimators of memory requirements (cache/memory hierarchy parameters) for applications executing on proposed architectures

5.9.2. Tools to allow the rapid comparison of competing DSP architectures and instruction sets in their implementation of algorithms expressed at a high level

5.9.3. Practical methods and tools to evaluate, track and partition requirements in heterogeneous, hierarchical application domains

5.9.4. On-chip performance, power and temperature measurement/monitoring hardware for adaptive control or post-silicon testing and measurement