SRC Integrated Circuits and System Sciences (ICSS)

Research Needs Document for 2002-2007

ICSS Science Area Coordinating Committee (SACC)

June 1, 2002

Purpose

This document outlines research needs for Integrated Circuits and Systems for a five to ten year horizon. The list was compiled as a joint effort by industry experts representing the Semiconductor Research Corporation (SRC) member companies, with guidance from the International Technology Roadmap for Semiconductors (ITRS). University investigators seeking research funding from the SRC Integrated Circuits and System Sciences (ICSS) program should target one or more of the key research areas outlined in this document, or as specified in an accompanying Call for Research.

Background

The SRC Integrated Circuits and Systems Science (ICSS) research program aims to:

- Pursue research opportunities in advanced integrated circuits and systems design, exploiting advances in IC technology while overcoming associated barriers
- Challenge conventional notions of the design space

ICSS research stresses innovative system design, design methodologies, and circuit design techniques for heterogeneous mixed signal systems featuring low power, embedded software, and high speed communications.

A major transition in integrated systems technology is underway, and over the coming decade, there will be profound changes in the way we think about and design these systems. Since the earliest days of integrated circuits and computers, silicon systems have been designed under the assumption that transistors will decrease in cost annually to the point of being essentially free. We have treated power consumption as a secondary concern until fairly recently. Communication bandwidth has always been treated as a scarce commodity. However, most technology forecasts today predict a major shift in this thinking: Long-haul communications bandwidth has recently

been estimated to be doubling every 9 months, much faster than Moore's Law; the availability of short range, low power communications technologies such as IEEE 802.11, Bluetooth and UWB has begun to explode, providing nearly "free" bandwidth availability for a large class of systems; and energy consumption has arguably become the primary limitation on further progress in design for many important classes of systems.

The development process for electronic circuits and systems has rapidly changed from the efforts of isolated individuals to joint, collaborative projects spanning the globe. In this highly distributed design environment, new design techniques and methodologies are required. Clear expectations must be defined and architectural tradeoffs made early in the design process. Products must be designed in an extremely short time, with no allowance for redesigns, in order to meet market demands

The new design environment and customer requirements are driving research on many fronts. The research needs outlined in this document are arbitrarily organized into classifications which correspond to the structure of the ICSS research portfolio. It is not intended that these classifications limit the span or scope of any proposed research. Proposals that encompass activity in any or all of these categories, or in related categories that are not explicitly stated, are welcome.

System Design

Note: The term "system" used in this document refers to systems implemented within a few semiconductor components, such as a System-on-a-Chip (SoC) or System-in-a-Package (SiP), implementing (for instance) a computing or communication processor. The term does not cover large-scale systems in the sense of (for instance) a cellular phone system or an automotive electronics system. Generally, we intend the term to encompass the kinds of products likely to be manufactured by SRC member companies over the decade 2002-2012.

S1: Algorithms, Applications, and Specifications

1. High level specifications of complex systems

   Examples:

   - Abstract, but executable, functional models
   - Performance models
   - Complex control specifications (algorithmic description and cycle-accurate description)
   - Architectural building blocks for computing and communication processors
   - Design constraints and requirements – analyzable, but not necessarily executable (cf. Rosetta)

2. Low-power, real time algorithms and architectures

   Examples:

   - Encryption/decryption
   - Real-time audio, 2D/3D video and data
   - Real Time Operating System (RTOS) architectures that support high levels of concurrent applications
   - RTOS synthesis (Schedulers and communication services) to support low power

3. High bandwidth and/or low power communications

   Examples:

   - Channel equalization methods: adaptive, continuous time, discrete time Finite Impulse Response (FIR), etc.
   - Ultra-wide-band communications schemes
   - Ultra low power RF links

S2: Architectures and Microarchitectures

1. High performance processor microarchitectures

   Examples:

   - Instruction-level and/or fine grain parallelism
   - Coarse grain parallelism (e.g. Advances in: superscalar, Very Long Instruction Word (VLIW), SIMD/Vector, multi-scalar, multi-threading, chip multi-processors (CMP), on-die memory hierarchy, etc.)

2. Adaptive or polymorphous processors

   Examples:

- Static and dynamically reconfigurable processors

3. Synthesizable communication or digital signal processor (DSP)

4. Deep sub-micron (DSM)-aware microarchitectures, accounting for noise, power, timing, interconnects, etc.

5. High performance audio and video stream processing

   Examples:

   - High performance processors to encode and decode data streams
   - Novel logic level building blocks for communication processors
   - Novel techniques to synthesize communications (DSP) processors from high level descriptions
   - Rapidly filed programmable communications processors to accommodate dynamically changing protocol and application needs

6. Novel system architectures enabled by the inclusion of non-traditional technologies

   Examples:

   - Optics and the use of III-V compounds such as InP and GaAs
   - Magnetic materials and structures
   - Embedded microstructures and microsystems: mechanical, electrical, and electromechanical (MEMS)
   - RF and microwaves
   - Organic compounds and materials
   - Other non-silicon based technologies

S3: System Design Exploration

1. Evaluation and Estimation of Architectural Paradigms

   Examples:

   - Memory requirement estimators for applications executing on proposed architectures
   - Tools to allow rapid comparison of competing DSP architectures and instruction sets
   - Evaluation of communication architectures

2. Early Design Space Exploration

   Examples:

   - System architects' design environment
   - High level design partitioning (HW/SW & HW/HW) and hierarchy
   - Early power/performance/area tradeoff and system level power reduction
   - Source-level behavioral transformations
   - Hardware pipeline scheduling and exploration tools
   - Leveraging physical design information (e.g., floorplanning) during microarchitectural design

3. Simulation and Early Verification

   Examples:

   - Very fast functional simulation

- Cycle accurate performance and power analysis
- Mixed-domain models and simulators (mechanical/electrical, analog/digital/RF/memory, HW/SW, etc.)
- Protocol verification to identify tricky control bugs

S4: System Level Synthesis and Optimization

1. On-chip communication

   Examples:

   - Global optimization of on-chip communication resources (for power/bandwidth/error performance)
   - Error-correcting on-chip networks for high bandwidth communications
   - Novel on-chip network/interconnect generation techniques
   - High-speed low-overhead on-chip signaling
   - Asynchronous, self-timed and multiple clock processing, with design tool support

2. High level synthesis to implementation

   Examples:

   - Design refinements/transformations from high level model to RTL
   - Approaches, such as platform-based design and extensions, for accelerating initial SoC integration and derivative generation from a high level description
   - Tools to efficiently compile algorithms and high-level models into hardware or software
   - Hardware synthesis of high quality, control-dominated designs
   - Techniques to synthesize communication processors (DSP) from high level descriptions
   - Innovative reusable library of building blocks optimized for DSP, general computing, and communication processors (low power, high performance, etc.)

3. Restructuring algorithms

   Examples:

   - Power reduction
   - Power/performance tradeoffs
   - Enhanced fault tolerance and/or reliability
   - Digital techniques to enhance analog circuit performance

4. Design for test

   Examples:

   - SoC level Built in Self Test (BIST)
   - Test architectures, and test interfaces

5. Chip-to-chip interfaces

   Examples:

   - Current mode chip-to-chip signaling

Circuit Design

Circuit Design research should emphasize the exploitation of advanced semiconductor technologies (not necessarily limited to silicon or CMOS) for high performance analog, digital, mixed signal, and RF systems, and avoidance of the undesirable side effects of technological advances. High level modeling and simulation, as well as physical realization and characterization, are strongly encouraged for all projects within the Circuit Design thrust.

C1: Digital Circuit Designs

1. Circuits on Advanced Technologies

   Examples:

   - Circuits that comprehend, manage, and possibly leverage the effects of large subthreshold leakage or large gate leakage currents
   - Adaptive, self-compensating circuits to combat local device and interconnect timing variations
   - Electrostatic Discharge (ESD) protection, device modeling and design.
   - Circuits on non-silicon based technologies
   - Multi-level digital logic

2. Low power and/or low voltage circuit design

   Examples:

   - Circuits immune and/or tolerant to soft errors
   - Noise tolerant, ultra-low-swing interconnects
   - Adiabatic circuit design styles
   - Leakage reduction techniques
   - Circuit research that is closely coupled to architectural innovations for developing low power scalable digital systems
   - Alternatives to aggressive voltage scaling to minimize power such as, but not limited to, noise-tolerant, ultra-low-swing logic schemes, adiabatic circuit styles, and the use of on-chip magnetics
   - Low noise digital circuits

3. High Performance Digital circuit design

4. Design for Manufacturability

5. Innovative on-chip interconnect scaling

   Examples:

   - On-chip communications
   - Signal bussing structures
   - Clock schemes

6. Advanced Power distribution

   Examples:

   - Noise decoupling

7. Innovative design approaches for Large Scale ASICs

   Examples:

   - Innovative memory structures and hierarchy
   - Skew tolerant synchronous circuits
   - Asynchronous circuits
   - Design for testability (DFT), BIST or otherwise.
   - Reconfigurable IP
   - Electromagnetic interference (EMI) reduction

C2: Mixed Signal/Analog/RF Circuit Designs

1. Circuits on Advanced Technologies

   Examples:

   - Circuits that comprehend, manage, and possibly leverage the effects of large subthreshold leakage or large gate leakage currents
   - CMOS RF building blocks for 1-10GHz
   - High-isolation, high-efficiency on-chip and chip-to-chip transmit/receive switches
   - Circuits on non-silicon based technologies
   - ESD protection of Analog/RF circuits
   - Mixed voltage design (I/O and digital vs. analog)

2. Noise immune and/or tolerant circuits

   Examples:

   - Substrate noise understanding

3. Design for test

   Examples:

   - Analog/RF BIST

4. Low power and/or voltage circuit designs

   Examples:

   - Low voltage analog blocks (power converters, data converters, OTA, references, etc)
   - Monolithic quadrature capable 1-10GHz Voltage Controlled Oscillators (VCOs)

5. Adaptive circuits

   Examples:

   - Mixed-signal/Analog/RF circuits that are adaptable using digital signaling

6. Circuits for high speed communication

   Examples:

   - High speed analog to digital converters

C3: Bridging Research

This classification addresses projects which potentially bridge between SRC Science Areas and thrusts. Research in these areas is likely to require coordination and management of projects by multiple SACCs.

1. Process and circuit development

   Examples

   - Process optimization of devices for low power circuit usage
   - RF circuit optimization in RF-BiCMOS

2. CAD and Circuit interactions

   Examples

   - Analog design reuse

3. Device and Circuit interactions

   Examples

   - MEMS devices for circuit design
   - Device modeling
   - Novel device structures for scaling and/or low power (FinFET, 3D integrated circuits, quantum devices)

4. Package and Circuit interactions

   Examples

   - Novel techniques for package modeling and its effects on circuit design
   - Active thermal management
   - EMI design

5. Semiconductor Materials/Processes and Circuit Design interactions

   Examples

   - Low leakage device design and circuit usage – novel process technology/circuit collaboration to break the barrier imposed by current process technologies.
   - Substrate modeling

Key Technologies

The System Design and Circuit Design sections above are broad listings of research areas of interest to the ICSS area of the SRC. However, the member companies have identified key technologies that are of critical importance for products in the 3-5 year timeframe for both the System Design and the Circuit Design thrusts. This section highlights these key technologies, listed in order of priority. Topics not listed here are of interest, and will be considered, but only to the extent that adequate funding has already been achieved on these Key Technologies.

System Design Key Technologies

S3.2: Early Design space exploration

S1.2: Low power, real-time algorithms and architecture

S4.1: On-chip communication

S1.3: High bandwidth and/or low power communication

S2.4: Deep sub-micron aware microarchitectures, accounting for noise, power, timing, interconnects, etc.

S1.1: High level specifications of complex systems

Circuit Design Key Technologies

C1.2: Digital Low Power and/or Low Voltage Circuit Design

C2.1: Mixed Signal Circuits on Advanced Technologies

C2.4: Mixed Signal Low Power and/or Low Voltage Circuit Design

C1.1: Digital Circuits on Advanced Technologies

C2.3: Mixed Signal Design for Test

C2.2: Mixed Signal Noise immune and/or tolerant circuits