ICSS Research Needs: Integrated System Design

The ITRS identifies **Design Cost**, due to exploding Silicon and System Complexities, as the key factor with the potential to limit the semiconductor roadmap. Automation of the design process has lead to quantum gains in design productivity, as exemplified by productivity boosts obtained through the automation of physical design and, a little later, by the full automation of logic design through synthesis. Unlike logic synthesis, higher-level synthesis will generally be application or design class specific while what is needed are automatic, optimized, and design target specific, HW/SW partitioning and translation, of high-level system descriptions into micro-architectures (RTL) that could feed well-established back end design flow. A companion need is for back-annotation of implementation level parameters (delays, current/power, area, cross-coupling between signals, reliability, etc) into the high level design, with appropriate models that can be calibrated to achieve adequate accuracy.

The ITRS also projects that beyond the 65nm node, on-chip communications will require new design approaches to achieve system level performance targets and to achieve global optimization of communications resources. Among the approaches proposed are GALS micro architectures, Interconnect-Exploitive and other Alternative Architectures, Systolic Architectures, Active Interconnects, Distributed and Highly Parallel Architectures.

One of the major concerns in Integrated System Design is power management and minimization. Traditional performance-power trade off techniques are inadequate to address future technology leakage power in a reliable manner. Novel global optimization techniques will be needed at *every* design step, top to bottom, to achieve the targeted solution.

Variability of technological parameters is a growing concern, as is reliability. Major emphasis is needed in the area of Design Robustness to address these issues. For instance, these needs include tools for analysis, reduction, and avoidance of coupling effects; statistical design tools and methods, for optimizing systems in which all components are nominally functional; and probabilistic design tools and methods for achieving acceptable functionality from systems in which some components are not functional, or which may fail either transiently or permanently.

	2004 Integrated System Design Needs Category
S 1-	**System Level Synthesis and Optimization: Early Design Space Exploration**
S 1.1	High Level Executable Specifications of Complex Systems
S 1.2	Evaluation and Estimation of Architectural Paradigms
S 1.3	System Level Verification methodologies and algorithms
S 1.4	HW-SW Co-Design
S 1.5	Re-Structuring Algorithms
S 1.6	Adaptive or Polymorphous Processors
S 1.7	Synthesizable Communications or DSP Processors
S 1.8	Algorithms and methods for quantifying performance-power trade off in early design steps with reasonable accuracy.
S 1.9	Algorithms and methods to analyze boundaries, and extreme usage conditions.
S 1-	**System Level Synthesis and Optimization: High Level Synthesis to Implementation**
S 1.10	Micro-Architecture Synthesis
S 1.11	Platform Based Design
S 1.12	High Level Executable Specifications of Complex Systems
S 2-	**Design Robustness**
S 2.1	Analysis Reduction and Avoidance of Coupling Effects
S 2.2	Statistical Design Methods: Optimizing Systems in which all components are nominally functional
S 2.3	Probabilistic Methods: Achieving acceptable functionality from systems in which some components are not functional, or which may fail transiently or permanently
S 2.4	Deep Sub-micron aware micro-architectures, accounting for noise, power, timing, interconnects, etc.
S 3-	**Communications Centric Design of SoC/SiP: Energy Efficient Communications**
S 3.1	On-Chip Communication
S 3.2	Chip-to-Chip Interfaces
S 3.3	Protocol Based Communications, Networks on a Chip
S 3-	**Communications Centric Design of SoC/SiP: Interconnect Exploitive and other alternate Architectures**
S 3.4	Locally Connected Architectures
S 3.5	Distributed and Highly Parallel Architectures
S 4-	**Algorithms and Applications**
S 4.1	Novel Coding Schemes for energy efficient communications
S 4.2	Adaptive Algorithms enabling low power communications through noisy channels
S 4.3	Low-Power Real Time Algorithms and Architectures
S 4.4	High-Performance Processor Micro-Architectures
S 4.5	Novel System Architectures Enabled by the Inclusion of Emerging Technologies
S 5-	**System Power Optimization**
S 5.1	Novel cache architectures: efficient and reliable leakage control for large arrays SACC
S 5.2	Efficient control of active power and elimination of hot spots
S 5.3	Reducing di/dt through smart compiling techniques
S 5.4	Novel scheduling of resources, balancing workload, optimizing micro code
S 5.5	Dynamic power management and optimization using novel distributed architectures
S 5.6	MCM and micro-architectures that support multiple power grids, multiple VRM, multiple system power states / clocks
S 5.7	Efficient power management to enable high performance, highly integrated, multi function SOC integrated multimedia, communication