ICSS Research Needs: Integrated Systems Design

The ITRS cites design cost due to exploding silicon and system complexities as the key factor with the potential to limit the semiconductor roadmap. These complexities are particularly notable given that ITRS predicts the practical end for CMOS scaling within a decade accompanied by increasing wiring resistances and extreme power densities. Thus, while creating the system function, designers must contend with all underlying technology challenges and physical limits. The 2006 needs categories were formulated in anticipation of these upcoming challenges and also recognizing that many design degrees of freedom are available for continuing the pace of system capability.

The 2006 update to the needs categories has been reorganized. Platform-based design (S2.2) is expanded to include mixed-signal/RF domains. Likewise, system-level implementation now includes S2.4, S2.5 and S2.6 to emphasize algorithm modeling, latency insensitivity and validations of performance and robustness of both hardware and software. Similarly, the section on design robustness now has S3.1 focusing on handling of systems designs in the context of significant subcomponent variations.

Design automation has lead to quantum gains in design capability and productivity; design cycle times have not grown as rapidly as the sizes of design tasks. However, while CAD is necessarily related to system design, the main objects of the 2006 needs categories are innovations in systems architectures and algorithms to execute high-level tasks within the context of technology capability. Any proposed CAD research must develop new capabilities in the context of a system design proposal. Proposals with CAD tools as their main deliverable are beyond the scope of this solicitation.

What is needed is automatic, optimized, and design target specific flow from high-level system descriptions into micro-architectures (RTL) that could feed well-established back end design flow. A companion need is for back-annotation of implementation level parameters (delays, current/power, area, cross-coupling between signals, reliability, *etc.*) into the high-level design, with appropriate models that can be calibrated to achieve adequate accuracy.

The ITRS also projects that as technology continues to scale, on-chip communications will require new design approaches to achieve system-level performance targets and to achieve global optimization of communications resources.

One of the major concerns in integrated systems design is power management and minimization. Traditional performance-power trade off techniques are inadequate to address future technology leakage power in a reliable manner. Novel global optimization techniques will be needed at every design step, top to bottom, to achieve the targeted solution.

Variability of technological parameters is a growing concern, as is reliability. Major emphasis is needed in the area of design robustness to address these issues. For instance, these needs include approaches for analysis, reduction, and avoidance of coupling effects; statistical design methods, for optimizing systems in which all components are nominally functional; and probabilistic design methods for achieving acceptable performance from systems in which some components are not functional, or which may fail either transiently or permanently.

2006 Integrated Systems Design Needs Categories	
S1	**Early Design Space Exploration for System Level Synthesis and Optimization**
S1.1	High level executable specifications of complex systems
S1.2	Evaluation and estimation of architectural paradigms
S1.3	HW-SW co-design
S1.4	Adaptive or polymorphous processors
S1.5	Synthesizable communications or DSP processors
S1.6	Algorithms and methods for quantifying performance-power trade-off in early design steps with reasonable accuracy
S2	**System Level Implementation**
S2.1	Microarchitecture synthesis
S2.2	Platform based design, component-based, composability, including analog/RF/mixed-signal sub-systems
S2.3	High level executable specifications of complex systems
S2.4	Algorithmic level modeling
S2.5	Latency insensitive design
S2.6	System level validations of performance and robustness including both hardware and software
S3	**Design Robustness**
S3.1	Design methods and architectures for systems using components with significant variations
S3.2	Design methods and architectures for systems in which some components are not functional, or which may fail transiently or permanently
S3.3	Deep sub-micron aware microarchitectures, accounting for noise, power, timing, interconnects, etc.
S4	**System Power Optimization**
S4.1	Novel cache architectures: Efficient and reliable leakage control for large arrays SACC
S4.2	Efficient control of active power and elimination of hot spots
S4.3	Reducing di/dt through smart compiling techniques
S4.4	Novel scheduling of resources, balancing workload, optimizing microcode
S4.5	Dynamic power management and optimization using novel distributed architectures
S4.6	MCM and microarchitectures that support multiple power grids, multiple VRM, multiple system power states/clocks
S46.7	Efficient power management to enable high performance, highly integrated, multi-function SoC integrated multimedia communication
S5	**Communications Centric Design of SoC/SiP: Energy Efficient Communications**
S5.1	On-chip communication
S5.2	Chip-to-chip interfaces
S5.3	Protocol-based communications, network-on-chip
S5.4	Design methodology for large numbers of parallel cores
S6	**Algorithms and Applications**
S6.1	Novel coding schemes for energy efficient communications
S6.2	Adaptive algorithms enabling low power communications through noisy channels
S6.3	Low-power real time algorithms and architectures
S6.4	High-performance processor microarchitectures
S6.5	Novel system architectures enabled by the inclusion of emerging technologies