ICSS Research Needs: Integrated System Design 2010

The SRC GRC member companies are pleased to release this document that describes their research needs in the thrust of Integrated System Design. Incorporated into this document are the Grand Challenges from the International Technology Roadmap for Semiconductors (http://public.itrs.net) as well as needs identified through the ICSS strategic planning process, workshops and joint discussions.

The ITRS cites design cost due to exploding silicon and system complexities as a key factor with the potential to limit the semiconductor roadmap. These complexities are particularly notable given that ITRS predicts that by the end of the next decade, new non-CMOS devices will be needed to augment the capabilities of the CMOS process, effectively marking the end of traditional CMOS scaling. Thus, while creating the system function, designers must contend with all underlying technology challenges and approaching physical limits. These needs categories were formulated in anticipation of these upcoming challenges and also recognizing that many design degrees of freedom are available for continuing the pace of system capability.

Design automation has led to quantum gains in design capability and productivity; design cycle times have not grown as rapidly as the sizes of design tasks. However, while CAD is necessarily related to system design, the main objects of the 2010 needs categories are innovations in systems architectures and algorithms to execute high-level tasks within the context of technology capability. Any proposed CAD research must develop new capabilities in the context of a system design proposal and have an emphasis on electronic system level descriptions and models. Proposals with CAD tools as their main deliverable are beyond the scope of this solicitation.

What is needed is automatic, optimized, and design target specific flow from high-level system descriptions into micro-architectures (RTL) that could feed well-established back end design flow. A companion need is for back-annotation of implementation level parameters (delays, current/power, area, cross-coupling between signals, reliability, etc.) into the high-level design, with appropriate models that can be calibrated to achieve adequate accuracy.

As technology continues to scale, on-chip communications will require new design approaches to achieve system-level performance targets and to achieve global optimization of communications resources.

One of the major concerns in integrated system design is power management and minimization. Traditional performance-power trade-off techniques are inadequate to address future technology leakage power in a reliable manner. Novel global optimization techniques will be needed at every design step, top to bottom, to achieve the targeted solution.

Variability of technological parameters is a growing concern, as is reliability. Major emphasis is needed in the area of design robustness to address these issues. For instance, these needs include approaches for analysis, reduction, and avoidance of coupling effects; statistical design methods, for optimizing systems in which all components are nominally functional; and probabilistic design methods for achieving acceptable performance from systems in which some components are not functional, or which may fail either transiently or permanently.

White Papers for all the categories below will be considered for funding. Please note the categories in bold were highlighted by member companies for this 2010 solicitation as being particularly valuable to the industry.

2010 Integrated System Design Needs Categories	
S1	**Early Design Space Exploration for System Level Synthesis and Optimization**
S1.1	**High level executable models of complex systems and their use for design and validation**
S1.2	**Algorithms and methods for quantifying performance-power trade-off in early design steps with reasonable accuracy**
S1.3	**Adaptive or polymorphous processors**
S1.4	High level exploration for systems utilizing 3-D packaging
S1.5	Evaluation and estimation of architectural paradigms
S1.6	Synthesizable accelerators
S2	**System Level Implementation**
S2.1	**System level validations of performance and robustness including both hardware and software**
S2.2	**Analog/RF/mixed-signal sub-systems, platform based design, including ultra low power applications**
S2.3	**Effective and fast turn-around design flows for SoC/SiP, including high performance IP blocks (e.g. processor cores)**
S2.4	**System architectures having access to significantly higher off-chip bandwidth (i.e. optical)**
S2.5	**Microarchitecture synthesis**
S2.6	**Algorithmic level modeling**
S2.7	Latency insensitive and elastic designs
S3	**Design Robustness**
S3.1	**Design methods and architectures for systems in which some components may fail transiently or permanently**
S3.2	**Design methods and architectures for correct systems behavior, even while using some non-functional components**
S3.3	**Deep sub-micron aware microarchitectures, accounting for noise, power, timing, interconnects, etc.**
S4	**System Power Optimization**
S4.1	**Efficient power management to enable high performance, highly integrated, multi-function SoC**
S4.2	**Novel cache architectures: Efficient and reliable leakage control for large arrays**
S4.3	**Efficient control of active power and elimination of hot spots**
S4.4	**Reducing di/dt through microarchitectural design and software techniques**
S4.5	**Novel scheduling of resources, balancing workload, optimizing microcode**
S4.6	**Dynamic power management and optimization using novel distributed architectures**
S4.7	**MCM and microarchitectures that support multiple power grids, multiple VRM, multiple system power states/clocks**
S4.8	Efficient analog architectures, including power amplifier applications
S5	**Multi-core SoC Design**
S5.1	**Design methodology for large numbers of parallel cores**
S5.2	**Design and validation of on-chip communication fabrics and protocols**
S5.3	**Chip-to-chip interfaces**
S5.4	Multicore programming for massively parallel signal processing, low power and real time systems
S6	**Algorithms and Applications**
S6.1	**Multi-core algorithms, coding, software tools and applications**
S6.2	**Virtualization for hardware and software systems**
S6.3	**Novel memory sub systems and architectures enabled by the inclusion of emerging memory technologies (i.e. EDRAM, ZRAM, e-Flash RAM)**
S6.4	**High-performance processor microarchitectures**
S6.5	**Novel system architectures enabled by the inclusion of emerging technologies**
S6.6	**Low-power real time algorithms and architectures**
S6.7	Adaptive algorithms enabling low power communications through noisy channels
S6.8	Smart grid applications
S6.9	Medical implantable applications
S6.10	Body area networks, mesh networks, sensor networks
S6.11	Algorithms for medical imaging applications including optical, ultra-sound
S7	**SW/HW Co-design and Co-optimization**
S7.1	**Optimizing SW-HW interfaces**
S7.2	**Dynamic scheduling and thread migration**
S7.3	**Communicating OS and application information to HW platform**
S7.4	**System level validation across SW-HW boundary**
S7.5	**Quality assurance and validation of firmware**