Integrated Circuit and Systems Sciences
Research Needs: Circuit Design
June 2013

The Semiconductor Research Corporation (SRC) Global Research Collaboration (GRC) program member companies are pleased to release this document that describes the research needs in the thrust of Circuit Design including that for Texas Analog Center of Excellence (TxACE). Incorporated into this document are the Grand Challenges from the International Technology Roadmap for Semiconductors (http://public.itrs.net) as well as needs identified through SRC GRC Executive Technical Advisory Board (ETAB) priorities, the Integrated Circuit and Systems Sciences (ICSS) strategic planning process, TxACE workshops and joint discussions.

The circuit design research needs of the members are described in six major categories:

- Circuit Power/Energy Management/Optimization
- Circuit Design Robustness (Analog, Digital, RF, and Memory)
- High Performance Circuits
- Circuits in Advanced and Emerging Technologies
- Bridging Research Across Disciplines
- Circuit Design for Emerging Applications

Each of these major categories is broken down into several sub-categories which describe the need in more detail. Even so, these are written to be broad in nature so as not to restrict the investigator's approach.

The needs in the circuit design space cover a broad range of applications, including high performance processors for data centers, low power processors for mobile computing and communication, healthcare devices, and efficient energy usage and management systems. Investigators are encouraged to link the results of their work with a potential application to help describe the relevance of the proposed work.

White Papers for all the categories below will be considered for funding. Note that there is no priority assigned to the order of the major categories or the sub categories. Investigators are limited to participation in two white papers in this Circuit Design solicitation. Submissions should highlight which needs are addressed, such as "C2.1".

CONTRIBUTORS

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Further explanation for C5, Bridging Research Across Disciplines: Device models are a critical interface between the underlying technology and integrated circuit design. Combined with circuit simulation tools, good device models significantly improve design productivity and provide insight into the relationship between design choices and circuit performance. Good device models should scale with latest technology advances, be accurate across a wide range of process / operating conditions, and be efficient. These modeling requirements are challenged by the lengthening list of alternative device materials, structures, and increasing process variations: (1) high-permittivity (high-k) gate dielectrics, (2) metal gate electrodes, (3) low-resistance source / drain, (4) strained channel for high mobility, and now (5) non-planar FinFETs and 3D packaging. Process variation usually manifests itself as parameter fluctuations in the transistor characteristics: typically (1) channel length / delay, (2) threshold voltage, and (3) transistor parasitics. One builds and characterizes appropriate test structures, accurately extracts, and then embeds these variations into a transistor model file. Only then can the circuit designer perform statistical analysis and optimization to try to mitigate performance variability. Rigorous extraction helps process development shed light on the mechanism of variations. The modeling challenge under variation is to identify systematic variation components, develop predictive models for performance analysis, and incorporate them into design tools.

Design rules not only act as a means to integrate IC design and manufacturing but also isolate the design and manufacturing communities from the challenges faced by the other. Design rules attempt to define these process limits in terms of overly simplified design constraints. Process development engineers have introduced additional design rules to account for failures that occur due to lithography, Chemical Mechanical Polishing (CMP), etch-loading, implant variation, stresses in dielectrics, and other complex physical, chemical, and mechanical interactions. In addition, the need for Resolution Enhancement Techniques (RET) in Optical Proximity Correction (OPC) compliant lithography friendly designs at the most advanced process nodes has further increased the raw number and complexity of these rules. Now Design For Manufacturing (DFM) has become mandatory and has introduced restricted design rules such as the use of a smaller range of critical line widths, unidirectional layout, on grid layout, and is moving toward extreme regularity which limits the number of unique standard cells and standard cell groupings. Memory and FPGAs have long employed regularity to address manufacturability challenges posed by new technology nodes. By limiting the number and arrangement of allowed shapes, one can afford extensive simulation, aggressive RET / OPC, and silicon verification for the smaller number of unique structures surrounded by the regular neighborhood of other cells. The efficient use of area plus performance, power, and cost are the challenges with this approach. Process development is facing many difficult choices due to the delay of EUV technology. Potential alternatives such as frequency quadrupling Directed Self Assembly (DSA) or double Self-Aligned Double Patterning (SADP) are dependent on extreme layout regularity to be successful. For lines and spaces, the trend is toward only 1 line width at 1 spacing that can be manufactured in 1 orientation. Device differentiation comes through a cut mask: gate length and pitch will be fixed; gate width will be adjusted by a cut mask. The “traditional” triple or quadruple patterning approach such as Litho-Etch, Litho-Etch, Litho-Etch (LELELE) faces severe alignment challenges, and given the number of critical masking layers, is not likely to be economically feasible. Regardless of the technology employed (including EUV), lithography, etch, implant, CMP, OPC, and silicon verification would benefit significantly from extreme regularity. The SRC is already supporting research across science area thrusts into many aspects of advanced technology: advanced material and process development, CAD and design rules for extreme regularity, 3D devices and packaging, and thermal / power measurement and mitigation to name a few. Integrated cooperation with the circuit design community is sorely needed.

2013 Circuit Design Needs Categories

C1	**Circuit Power/Energy Management/Optimization**
Interest in circuits for power/energy management and optimization spans several orders of magnitude in power and energy. Challenges exist at all levels from data centers, racks, line cards, desktops, laptops, mobile processors all the way down to circuits in embedded microcontrollers consuming micro-Watts of active power and nano-Watts of leakage power. Novel circuits are desired for deeply scaled CMOS devices to improve the state of the art in both active and static current consumption along with management of thermal limitations. On the other end of the power spectrum in the ultra-low powered battery driven or energy harvesting application space, challenges remain in key areas such as power/performance scalable analog (ADC's, DAC's, Voltage Comparators, etc). An example would be an analog to digital converter capable of variable precision conversion with power scaling with the conversion precision. Crystal oscillators and oscillator interfaces needed for accurate time references consume much of the standby power for ULP devices that must wake up on specific time intervals to communicate with mesh networks or perform specific tasks on a schedule. ULP low ppm drift time or frequency references are needed. Another key ULP need is for CMOS nano power current sensors for coulomb counting. Nano power current sensors would have many uses such as voltage regulator or voltage converter control or to monitor and control current consumption into various power domains.	
C1.1	Very energy efficient digital and analog circuits
C1.2	High efficiency integrated (e.g. SoC, SiP, 3D) circuits used for power management, including regulators, DC DC converters, and controllers
C1.3	Thermal management circuitry including high accuracy compact temperature sensors
C1.4	Control/management of leakage current
C1.5	Ultra low power frequency or time sources (ppm drift rates suitable for real time clock applications)
C1.6	Nano-power current sensor for digital coulomb counting
C1.7	Power/performance scalable analog circuits
C1.8	Fine-grain power management techniques such as state-retention, rapid on/off, etc.
C2	**Circuit Design Robustness (Analog, Digital, RF and Memory)**
Across the disciplines of analog, digital, RF and memory circuit design, the most traditional way to build robust circuits has been through overdesign; most designs overachieve on the highest priority metrics (usually speed) when process and environmental parameters are nominal, so that those metrics still meet the desired specs even when degraded by variation in those parameters. The price of this overachievement is relaxation of lower priority metrics, usually power. Historically, steady improvement in the tradeoff between performance, area, and power has, however, slowed, while the desire for progress in function/power is as great as ever. At the same time, as supply voltages have become lower and integration has increased, worst-case variability of device parameters has become more noticeable. In recent years, robustness has increasingly been sought by making circuits tolerant to built-in and environmental effects with less overachievement at nominal conditions. Continued innovation is needed in the design of robust circuits. Member companies are seeking approaches that are robust under variation in global and local process conditions, under hard or soft failure of individual components, and under the impact of noise and ESD.	
C2.1	Circuits for increased tolerance and adaptability to manufacturing/process variability
C2.2	Increasing reliability by design with unreliable components, soft errors and voltage “overstress”
C2.3	Noise tolerant and aging tolerant circuits/isolation techniques, robust and low- capacitance ESD
C3	**High Performance Circuits**
In the "High-Performance Circuits" category high speed communications links, adaptive /high performance power efficient circuits, high speed interconnects continue to be important needs for members companies. For high-speed I/O, member companies seek a broad array of proposals that are not only ADC-based, but also use non-ADC designs with the goal of meeting high line rates (> 25Gb/s) and low power (<1pJ/bit) while being area efficient. An important component aspect of these designs is also the power-efficient DSP logic which is usually the critical path and not just the front-end ADCs. Proposals are also being sought for optical I/Os, and packaging and interconnect topologies in this domain. Scalable, area efficient, high-performance analog and RF circuits continue to be important with a need for configurable and modular architectures that enable reuse. Another addition to the needs document is on high-speed short distance wireless circuits which operate at low power. Proposal that target peak-efficiency of 1-2m with up-to a 10m range, 20-30Gb/s, low BER, and <10pJ/b power consumption are being sought. Another new need is the design of process-scalable high ENOB, interference aware RF ADC designs for applications such as 5G cognitive radio by pushing most of the signal processing to the digital or software realm to enable scaling.	
C3.1	On-chip interconnect scaling, including high-speed signaling techniques and interconnect driven design techniques

C3.2	Energy efficient high-speed communications links (<1pJ/bit @ >25Gbps)
C3.3	High-speed short-distance wireless circuits at very low power (e.g., 1-2m distance, 20-30Gb/s, <10pJ/bit power, low BER)
C3.4	Adaptive analog, digital, and memory circuits for improved power performance efficiency
C3.5	Power efficient high performance digital circuit design
C3.6	Power efficient, low jitter clocking circuits, including voltage scaling, multiple clock domains, and asynchronous/GALS
C3.7	High dynamic range analog front-ends for sensors
C3.8	Configurable modular analog and high-speed I/O architectures that improve reuse in SOC products
C3.9	Digitally enhanced analog/RF circuits
C3.10	Scalable High Resolution interference aware RF ADC for applications such as 5G cognitive radio
C4	**Circuits in Advanced and Emerging Technologies**
This category highlights the need for circuit design in advanced and emerging process technologies especially that enable aggressive process scaling into the sub-10nm range, 3D integration, and use of advanced CMOS structures. In the design of analog and RF circuits emphasis should be placed on scalable designs that enable transition down the technology node while ensuring that area scales proportionally. This will likely require the use of digital techniques to enhance the performance of the analog and RF. New volatile or non-volatile memory designs are also required while meeting the requirements of performance, power, reliability, and scalability. Circuit designs that utilize emerging memory technologies are also desired. Finally, circuits that are based on compressed sampling techniques are also a need.	
C4.1	Area efficient analog/RF design in scaled “digital” technologies
C4.2	Emerging memory design (volatile or nonvolatile) – high performance and power tradeoffs with high reliability and/or 3D scalability
C4.3	Digital circuits with low I_{on}/I_{off} in low head room CMOS processes (e.g. extreme scaled CMOS or high Vt ultra-low power)
C4.4	Low voltage digital and analog circuit design including moderate inversion and weak inversion regions of operation
C4.5	Circuit design techniques with advanced CMOS device structures
C4.6	Reconfigurable Analog/RF design in processes with non-volatile memory bits/tunable devices
C4.7	Robust, low power interface circuits for 3D integration
C4.8	Test structures that target characterization of new sources of variability, (e.g. FinFET devices, FDSOI, and 3D, etc.)
C4.9	Low power logic and circuit design utilizing emerging nonvolatile RAM memory technology
C4.10	Silicon circuits based on quantum principles
C4.11	Low power scalable circuits using compressed sampling technology for application such as wireless sensors
C5	**Bridging Research Across Disciplines**
Continued device scaling faces many issues: (1) increased susceptibility to soft errors such as energetic particle strikes, signal and power-supply noise coupling, and erratic device behavior, (2) hard errors from phenomena such as electromigration, device wear out, and aging (e.g. oxide breakdown, NBTI), and (3) for analog devices, gain decrease, reduced matching, and thermal sensitivity. In all, susceptibility to small fluctuations in the manufacturing process rises dramatically. From the manufacturing side, what actually appears on the wafer is becoming more of a suggestion of what was designed into the GDS. The days of What You See Is What You Get (WYSIWYG) are gone. Solving these issues requires a cross disciplinary approach involving close cooperation between the design, CAD, test, modeling, and process development communities. Operating as isolated silos of expertise is no longer sufficient to address the complexity and find compromises necessary to advance circuit design and the underlying technologies.	
C5.1	Semiconductor materials/processes/device and circuit design interactions/co-development, including novel non-CMOS devices, as well as extreme layout regularity
C5.2	Variation-aware device and interconnect modeling in advanced technologies
C5.3	Package and circuit interactions – high frequency, low noise, EMI management, power delivery, and 3D IC heat & temperature management
C5.4	Improved digital and/or analog circuit design optimization and productivity through novel CAD techniques, for example, utilizing data mining of process, test, and circuit analysis databases
C5.5	Mixed-signal isolation technologies for SoC, SiP and 3D
C5.6	Variation-aware and scalable analog/RF/memory/mixed-signal BIST/DFT circuits

2013 Circuit Design Needs Categories, continued

C6	Circuit Design for Emerging Applications
There is a need to focus on circuit design driven by several emerging applications. For example, in mixed-signal VLSI circuits, there is a growing need to operate in the millimeter wave and sub millimeter wave frequency regime, as well as very wide bandwidth range where design methodologies are immature, thus radical new ideas are needed to develop design capabilities. There is also a need to looking at novel sampling approaches including sub-Nyquist and compressive sensing techniques. Some of these needs are driven by software defined radios and cognitive radios, multi-band multi-standard infrastructure, cellular, connectivity and sensor networks. Similarly, on the ultra-low power side, there is a need to develop circuit techniques that could efficiently utilize low-bandwidth and low-duty cycle operation of sensors to reduce the power consumption down to bare minimum to be powered by energy harvesting circuits. Some of the applications include wireless health monitors, sensors, lighting, display and motor control. There is a need to look at low-power circuits for RF synchronization and hand shaking methods including wakeup radios, reliable energy efficient wireless power transceivers including antenna and techniques to manage multiple energy sources that may not be well behaved, such as energy harvesting sources. Finally, an additional emerging application need is the area of security with circuits for anti-counterfeiting, random number generation and secure operation.	
C6.1	Low power and scalable non-Nyquist and other novel sampling techniques (e.g. compressive sensing)
C6.2	Wearable health monitors: Power efficient body sensor circuitry and/or dry skin contact sensing
C6.3	Efficient and affordable circuits for emerging lighting and display applications
C6.4	Reliable energy efficient wireless power transmit and receive circuits, including the antenna
C6.5	Low power circuits for timing and control of sleep/wake sequences
C6.6	Circuits for managing multiple energy sources that are not well behaved, such as from energy harvesting
C6.7	Energy Efficient Spectrum Sensing for cognitive radio applications
C6.8	Circuits for multi-band/multi-standard, including front-ends (infrastructure, cellular, connectivity or wireless sensor network)
C6.9	Low-power circuits and techniques for RF synchronization and hand shaking including wakeup radios
C6.10	Signal amplification near and beyond f_{max} for millimeter wave and sub millimeter wave applications
C6.11	Energy efficient motor control and driver circuits
C6.12	Circuits for millimeter and sub-millimeter applications such as IR imaging and radar
C6.13	Low power circuits and applications utilizing time-based processing
C6.14	Anti-counterfeiting circuitry based on PUF and/or non-PUF techniques
C6.15	Standard process compatible true random number generation
C6.16	Circuits for side-channel attack detection and/or prevention