Back End Processing (BEP) Needs Statement

I. Introduction-

The purpose of this document is to define the needs of the SRC member companies in the area of Back End Processes (BEP), and to highlight specific areas where the SRC program will focus. In a proposal selection process, consideration will be given to the facilities required for research in specific areas, the compatibility of problems with the university environment and time scale, and the work being done in industry and at other consortia. In this document BEP is defined to include all of the processing and materials associated with providing on-chip interconnect and also novel design and process approaches to improve interconnect performance, including chip-package co-design.

II. Background

Progress in BEP is of critical importance to meet the roadmap requirements of future generations of ICs. As the performance scaling of IC device structures becomes increasingly difficult to achieve, it is expected that significant industry pressure will focus on accelerated interconnect performance to meet future IC requirements. The 2003 International Technology Roadmap for Semiconductors, however, has identified global wiring scaling issues as a major roadblock at the 45nm node and beyond. RC delay is dominated by global and semi-global interconnect. Historically the on-die interconnect delay has been increasing exponentially while the transistor delay has been decreasing exponentially. While the use of transistor repeaters, reverse scaling and interconnect based design can help mitigate the interconnect limitations, they do not provide scalable low power and high signal bandwidth solutions. In the near term, challenges include developing and integrating new materials to meet conductivity and dielectric permittivity requirements. In the longer term the major challenge is to identify when alternatives or additions to on-chip metal/dielectric interconnects will be needed for global interconnect, and what the acceptable alternatives can be. The solution to the global interconnect problem and the extendibility of copper / low-k interconnect to increasingly small lines and spaces are the major challenges faced by BEP.

It is now widely conceded that process technology alone cannot solve the global interconnect problem in the short term, and probably not in the long term. Rather, the current view is that design, process technology, and packaging must all converge to provide an optimized solution for interconnect requirements. The current projection is that near term interconnect delay problems in new ICs will be met by circuit design within the constraints of planar technology with special attention to minimizing the lengths of critical paths and increasing the use of repeaters. This will be done in concert with a substantial push in Cu/low-k technology, as well as more innovative packaging and board approaches, to minimize design architecture changes while still meeting the continued advances in performance dictated by roadmap projections.

In the intermediate term, Cu/low-k will be pushed to its limits, and new design architectures as well as chip-package co-design will be achieved with new CAD tools to significantly facilitate needed performance advances. Beyond these extrapolations of

current practices, radically new design, packaging, and technology options will be needed. Among the design options being considered are items such as non-synchronous clocking, interconnect-centric architectures and design tools, and interconnect aware verification and analysis. The packaging community is expected to impact the global interconnect problem in the near term with optimized co-design of the chip and package interconnects. In the longer term, innovations such as wafer scale packaging and package intermediated intra- and inter-chip interconnects will become available to alleviate the interconnect problem. Many new technology options are envisioned beyond the immediate Cu-low-k and IC/package redesign. Among these are optical interconnects, microwave/wireless interconnects, package intermediated interconnects (beyond simple package/IC co-design -- such things as multichip packages, active substrate packages, etc.), RF package coupled interconnects, 3D ICs, optical interconnects and nanotubes. Other futuristic approaches such as self-assembled interconnects and quantum communications via spin are intriguing concepts, but key advances and practical demonstrations are still needed to take these approaches much beyond the speculation stage.

Each of the approaches listed above has the potential to make significant inroads to minimize the problems associated with global interconnect. In addition, there are opportunities for process technology breakthroughs that will extend the capabilities of conventional Cu/low-k interconnects. Researchers in all areas have not only the responsibility to advance the state of the art, but also to maintain coordination to insure that capabilities being developed in one area are not antiquated by advances in other research activities.

SRC member companies identified two BEP areas of critical importance for continued progress in the semiconductor industry: the extendibility of Cu/Low-k interconnect technologies and novel solutions to the global interconnect problem. The BEP targets and solicits research in these areas as described below.

III. Needs:

Each of the options for advanced interconnect technology described above has significant additional research and development required to make it feasible for implementation at SRC member companies. Table 1 highlights the specific needs identified by the SRC member companies in the BEP thrust area. (Appendix 1 provides an overview discussion of the specific needs.)

Table 1 – BEP Thrust Area Needs

Thrust Area	**Need**	**Desired Research Areas**
Cu/Low-k Extendibility	Metallization Maintaining low resistivity throughout the technology nodes	Deposition Diffusion barriers Seed Layers Alternative materials
	Dielectrics Achieving K_{eff} targets	New Materials Deposition/Curing Pore sealing Modeling Pore formation & microstructure Barriers
	Etch/Plasma	Dielectric/Low-k damage Fundamentals End-point detection Diagnostics
	Planarization	Improved CMP Novel Planarization Abrasives
	Surface Preparation/Cleans	Damage free cleaning Annealing/curing damage Modeling
	Metrology	High-aspect ratio capability Porous low-k Void detection In-situ and in-line
	Modeling/Simulation	High Frequency systems >2GHz Design optimization Heat dissipation/thermal Optical systems
	Reliability	Predictive Modeling Characterization Accelerated testing techniques Stress/thermal effects
	Fundamentals	Fundamental limits Cu/Low-k interactions Barriers/diffusion Film growth Thermal effects/grain boundary growth
Novel Interconnect Solutions	3D Interconnect	Integration Manufacturability Reliability Testing Thermal Management Modeling
	Microwave/RF Interconnect	Integration Manufacturability Reliability Testing Thermal Management Modeling
	Optical Interconnect	Integration Manufacturability Reliability Testing Thermal Management

		Modeling
	Radical Alternatives	Proof of concept Modeling

IV. Challenges in Novel Interconnect

The Interconnect segment of the 2003 ITRS defines five difficult Interconnect challenges beyond 45nm and beyond the year 2009. These challenges include mitigating the impact of size effects in interconnect structures on performance, dimensional control; patterning, cleaning and filling of nanoscale feature, integration of new processes and structures, and identifying solutions which address global wiring scaling issues. Meeting these challenges, as well as others in the BEP area, for future generations of ICs is a daunting task. Although some potential solutions are being pursued to meet these challenges (as noted above in Novel Solutions), at this time there are no clearly defined approaches that will meet the needs beyond 45nm and that are also easily extrapolated to further-out roadmap nodes. Although searches for the "perfect solution" to the interconnect problem that will suffice for all time are probably futile, it is imperative to continue to look for new concepts and radical alternatives that will meet the needs for several generations into the future, particularly in dramatically reducing power consumption and latency.

Since the "Challenges" portion of Needs is a search for yet undefined alternatives, no clear research directions can be established. It is possible, however, to look at some ongoing investigations and comment on their possibility to satisfy Novel Interconnect Solution needs. At the present time, some the optical interconnect and nanotubes programs that have been supported by the BEP Thrust fit into this category. In addition, some of the Global Interconnect sub-thrust within the Packaging Thrust clearly falls within the scope. Additional research areas, such as 3D, have components that fall into the regime of Novel Interconnect Solutions for BEP, even though much of the work in wafer bonding and via etching is now at the development stage. Many of the above mentioned areas are also topics being pursued by the MARCO Interconnect Focus Center. Because of this, the BEP Thrust plans to closely coordinate with the work going on within the Focus Center, and to drive the BEP work towards more innovative and more risky potential solutions to the long-range problems.

Many of the problems associated with extending the various concepts noted in the previous paragraph may, at some time, fit into the topics covered in earlier sections of this document. The Novel Interconnect Solutions sub-thrust is intended to be reserved for truly innovative and novel approaches. Because of this intent, programs in this sub-thrust will be funded as traditional contracts as well as small grants to explore and flesh out seminal thoughts. In many cases it is expected that the small grants will transition to full contracts in the other BEP sub-thrust areas.

Appendix 1 - Detailed BEP Needs

I. Overview

The purpose of the back-end-of-line (BEOL) interconnects is to provide power, ground, clock and signals throughout the semiconductor chip. Today, high performance designs use up to 10 levels of metal to accomplish these tasks. At future technology nodes with current approaches, even more levels will be required as raw gate densities continue to increase. While more levels are possible at further technology nodes, new technologies such as microwave interconnects or optical interconnects are expected to alleviate the need for these increasingly costly levels of metal.

According to the 2003 ITRS, alternate conductors and novel interconnect techniques may not be available until sometime after 2010. Until then advances in performance will be achieved primarily by modification of designs and various packaging schemes. The extent of modifications required, and the ensuing cost, will be critically dependent on the RC properties of metal/dielectric systems available. Therefore, the ability to extend the performance of copper and low-k films for semiconductor interconnect layers is crucial to the near term success of the industry.

Many challenges must be overcome to extend the use of copper and low-k dielectrics beyond the 45nm node. As the industry scales past the 90nm technology node, interfaces begin to dominate the BEOL, in terms of providing mechanical integrity of the structures, promoting or inhibiting interactions between adjacent layers, and providing preferred paths for atomic transport. Understanding and minimizing the impact of electron interface scattering effects on the resistivity of thin copper lines becomes crucial as the feature sizes approach the electron mean free path. Also, the reduction and/or elimination of copper diffusion barriers used in today's copper damascene technologies must be realized to minimize the effective resistance of the thin copper lines. Metal fill of high aspect ratio structures must be realized to continue to use damascene technology.

As barrier thickness scales with metal width to meet conductor effective resistivity goals, copper containment becomes increasingly more problematic, and eventually new copper passivation techniques and/or diffusion-resistant dielectrics are needed to provide essentially "zero thickness" solutions.

The effect of surface scattering on Cu resistivity, basically an interface effect, has been shown in Cu lines as large as 90nm. Even if these effects are reduced to acceptable levels by surface passivation treatments during device fabrication, they must be proven stable for long-term reliability considerations. The fundamental reliability limits of copper/low-k metallization must be identified to assess technology extendibility in these ranges, and to identify any unique failure modes that may arise.

Unit processes in Cu beyond the 45nm node demand an understanding of the fundamentals of Cu deposition, planarization, and annealing. CMP with minimization of erosion and dishing become even more important as dielectric thicknesses are scaled and low-k dielectrics with low density and poor mechanical strength are introduced. Being able to simultaneously model dielectric behavior, mechanical strength and

thermal properties of materials will be critical to unit process development. Likewise, these unit processes have corresponding challenges in metrology, etch, and in-line monitoring.

New, lower dielectric constant interlayer dielectric materials must be introduced to reduce line-to-line and level-to-level capacitance. These films must withstand the mechanical and chemical stresses characteristic of subsequent integration processes, such as those found in planarization, patterning, thermal excursion and packaging, without cracking or delamination, while maintaining the desired film properties. To reduce the effect of integration damage on these ultra low-k materials, new planarization techniques and low thermal budget processes may be required. The fundamental understanding of the effect of plasma processing on these low-k, porous materials also must be understood for successful integration, and the ability to dissipate heat generated by the active devices will become more difficult.

Low defectivity and tight dimensional control are critical for successful extension of copper and low-k beyond the 45nm technology node. In-situ and ex-situ metrology with the ability to measure sub 100nm features, films, or particles only a few molecules thick and with very high aspect ratios will be needed. Advanced process control using new in-situ analytical techniques will be necessary to control film properties of future copper and low-k interconnects. Also, with the reduction in dimensionality will come severe issues associated with reliability in terms of sustainable current density, resistance to thermal cycling, long-term mechanical degradation and perhaps evolution of as yet unknown exposures.

Control of high-aspect ratio technologies challenges all metrology methods. Key requirements are void detection in copper lines and pore size distribution in patterned low-k. Rapid in-line observation of a very small number of voids/larger pores is needed. Critical dimension measurements are also required for very high aspect ratio structures that are made from porous dielectric materials and require three-dimensional information for trench and via/contact sidewalls. These measurements will be further complicated by the underlying multi-film complexity.

Reference materials and a standard measurement methodology are required for new thin films such as interconnect barriers and low-k dielectric layers, and other processes. A measurement methodology is needed for complex material stacks and interfacial properties including physical and electrical properties. Further high frequency dielectric constant measurement advances are required.

The relationship between the fundamental material properties and the interconnect design requirements is a critical need for extended use of copper metallization in integrated circuits, similar to the j_{max} and “critical length” characteristics of traditional interconnections. This understanding is essential to ensure operation at higher current density and higher operating temperature. Higher levels of modeling will be required for designers to connect particular degradation modes with interconnect design layout to improve predictability and reduce susceptibility prior to initial chip fabrication to optimize the development cycle time.

One or more alternate interconnect approaches, such as optical interconnects, package intermediated interconnects, 3D interconnects, or microwave interconnects are expected to be used to address the challenges associated with scaling global interconnects. Although it is too early to know the full integration scheme for these approaches, and also too early for complete reliability investigations, an understanding of the reliability requirements and projected reliability performance is a critical consideration for alternate interconnect process and design selection.

Not all back end challenges will be solved by using new materials. The success of extending copper and low-k materials will also depend on novel integration and design concepts. Signal integrity and reduction of cross talk may be aided by introduction of new materials, but the ability to proactively integrate and design to minimize these issues up front is critical to extending our current method of back end of line integration. Sophisticated modeling and validation to understand complicated wiring paths is therefore necessary to design for success. Advanced concepts and corresponding design tools that consider the chip and the package as a single system with technology parameters as design variables are critically needed.

II. Cu/Low-k Extendibility

Specific tasks of interest to BEP that enable the extendibility of Cu/Low-k beyond the 45nm node are outlined below.

II.A Metallization:

- Highly conductive, thin, highly conformal barrier and seed layers.
- Advanced barrier materials and deposition techniques to engineer the smoothness and other properties of the Cu barrier interface to ameliorate the expected Cu resistivity increase caused by electron scattering effects.
- Alternate materials and fill techniques for high aspect ratio contact structures that would allow simplification of the current contact/barrier/conductor film stack.
- ECD and/or barrier processes to eliminate the need for a Cu nucleation layer.
- Techniques to fill lines and vias, including seedless plating, electroless plating, plating on ultra-thin seed, additive-free plating, or new electroplating techniques. Novel techniques for additive monitoring and control. Fundamental understanding of the effects of impurities in the metal or at barrier/dielectric interface on conductor microstructure, electromigration, stress migration and resistivity.
- Understanding of thin barriers with regard to interactions with low-k materials and electromigration. Develop a model that shows how barriers can be designed, clearly distinguishing between conducting and non-conducting barriers and their requirements.
- New processes and materials for passive devices within the interconnect structure, such as electrodes for metal-insulator-metal (MIM) capacitors to improve yield and reliability, or magnetic materials with different inductor designs to reduce the area of these devices.

II.B Dielectrics

- Low-k materials capable of achieving the minimum effective permittivity (k_{eff}) possible, for maximum device performance at a viable performance/price ratio, for Cu dual damascene technology
- Air-gap approaches including an understanding of dielectric breakdown at small spaces.
- Ultra-thin, low permittivity dielectric barriers.
- Porous Low-k dielectrics with bulk-like materials properties (hardness, modulus, thermal conductivity)
- Fundamental understanding of microstructure requirements for porous dielectric materials with respect to pore size, pore shape, aspect ratio and degree of interconnectivity (open versus closed).
- Sidewall pore sealing techniques compatible with dual damascene patterning and industry-standard ALD barrier deposition techniques and materials. Techniques to predict k value and modulus from chemical structures.
- Models to design an ideal dielectric film.
- Techniques to evaluate dielectric damage during film deposition and integration into Cu/low-k interconnects;
- Sidewall damage metrology, capable of better than 10nm resolution.
- Moderate (k>20) to high (k>100) permittivity materials and manufacturing processes capable of achieving continually higher density for decoupling and (MIM) capacitors.

II.C Etch/Plasma

- Fundamental understanding of plasma-surface interactions for low-k etch, ash, conductor deposition, and dielectric deposition applications.
- "Designer" plasma chemistries with advanced quantum chemistry and collision physics methods.
- Techniques to detect etch induced damage and/or residues on the sidewalls and interior of low-k films and on electromigration performance
- New in-situ endpoint detection approaches suitable for dual damascene approaches.
- Plasma and surface diagnostics.
- Better sensors for chamber conditioning and plasma properties.

II.D Planarization

- CMP and planarization techniques for metal-free isolation between deep sub-100nm spaced lines. Processes and metrology in post-CMP cleans for good electrical isolation.
- Research on novel copper planarization process for low modulus low-k materials and very thin barriers.
- Alternative metal/dielectric planarization techniques such as Chemically Enhanced Planarization (CEP), electropolishing, and Electro-chemical-mechanical polishing (ECMP) for improved productivity, erosion and 3D feature control, and for low stress compatibility with weak/porous dielectrics.
- New abrasive materials and chemistries with engineered chemical-physical properties and engineered pad materials to enhanced precision and defect performance in polishing processes.

II.E Surface Preparation/Cleans

- Novel surface conditioning and surface cleaning approaches for porous, carbon-containing ultra low-k dielectrics integration. Surface preparation and cleaning techniques beyond wet and plasma cleaning, such as supercritical fluids, cryogenic aerosols, and laser cleaning
- Develop novel wet or dry clean techniques to remove etch induced damage and residue on low-k films

II.F Metrology

- New techniques to measure pore size, distribution and connectivity of pores in low-k dielectrics.
- Techniques for measuring pore sealing on patterned wafers Control of high-aspect ratio technologies such as dual damascene.
- Void detection in copper lines and killer pore detection in patterned low-k.
- Measurement of complex material stacks and interfacial properties including physical and electrical properties.
- Manufacturing metrologies where device and interconnect technology remain undefined.

II.G Modeling/Simulation

- Modeling, simulation and validation of metal dielectric systems generation and performance at frequencies > 20GHz
- RLC capable for >20GHZ Cu/low-k operation and for systems using RF or TeraHz wave interconnections. Modeling, simulation and experimental validation of novel interconnect solutions, such as optical, RF and 3D interconnects.
- A means to optimally place function blocks for 3D integrated circuits on individual die and on die stacks.
- New models to optimize optical interconnect systems that include emitter and detector latency.
- Predictive thermal models that can accommodate thermal impacts of RF standing waves, the multiple heat generating layers embedded in a 3D IC, and heat generated by as well as thermal performance of optical devices and quantum well devices.

II.H Reliability

- Models that show the interaction of copper, barriers and dielectric films regarding stress and its effect on process induced voiding, stress migration and electromigration including the effect of scaling and dielectric modulus.
- New methods that characterize the reliability of large interconnect systems
- New methods that factor in joule heating from Low-k materials with low thermal conductivity.
- New modeling methods to connect reliability models to complex interconnect layout for predictability.
- Techniques to address reliability issues associated with packaging and low modulus low-k dielectrics.

- AC EM – modeling and experiments that include understanding failure mechanisms in Cu interconnects under non-DC test conditions (pulsed DC, bipolar AC) and evaluation of recovery coefficient for Cu.
- In-situ observation of EM void nucleation and growth during EM tests (such as using HVSEM)
- An understanding of the influence of stress conditions (time, temperature) during EM tests on Cu microstructure (grain growth/texture).
- Radiotracer techniques to establish copper's migration path in Cu/low-k interconnects.
- Methods to improve electromigration and stress migration resistance.

II.I Fundamentals

- Theoretical and experimental understanding of the fundamental limits of the material structures such as conductivity limiters, electron scattering at surfaces, microstructure and grain boundaries as a function of temperature, and electromigration of fine lines.
- Fundamental understanding of interconnect metal/dielectric interactions, particularly for new low-k dielectrics, copper and barrier materials
- Invention and integration of new materials for emerging technologies to replace conventional wiring based electronics with alternatives, such as RF, optical and bio based interconnect.
- Crosscut studies aimed at model/simulation module integration.
- Cross-cut studies looking at predicting film growth or etch performance

III. Novel Interconnect Solutions – New Concepts and Radical Alternatives

Novel interconnect solutions refer to solutions that are non-evolutionary, i.e. go beyond conventional Cu/low-k/repeater strategies for global interconnects or the passive backside heat sink for power dissipation. It is important to note that these novel solutions must eventually be both cost-effective and capable of high yield.

Three of the major interconnect issues for which evolutionary approaches look inadequate are the global interconnect problem, heat extraction, and material synthesis. More specifically, the transmission of global signals across an increasing die size with increased R and C from scaled interconnects is becoming more difficult to achieve in a small fraction of an ever decreasing clock cycle The extraction of increased power densities through interfaces which include porous low-k materials is challenging both device reliability and performance. The ability to synthesize materials from a specification of desired physical and electrical properties is a critically needed capability to eliminate the costly exploration of the wide variety of material options available for interconnect uses.

The heat extraction problem may be approached from many different perspectives, i.e. increasing the thermal conductivity on die with specially designed passive or active thermal paths, providing for effective heat extraction from both the front and backsides or inexpensive off die active cooling to replace forced air/heat sink approaches.

Microwave interconnects, package-mediated interconnects (such as multi-chip packages, active substrate packages, etc.), RF package coupled interconnects, 3D ICs, optical interconnects, and nanotubes are some of the new technology options envisioned beyond the immediate Cu/low-k and IC/package redesign. Other futuristic approaches such as self-assembled interconnects and quantum communications via spin are intriguing concepts, but will require major innovations to be useful in circuit applications.

3D interconnects comprise multiple levels of active devices stacked on top of one another to minimize the distance required for interconnects. The stacked layers may be separate chips that are connected through the package by conventional bond pads, may be separate chips bonded with innovative “through wafer” contacts, or multiple stacks of active devices in the interconnect layers on a single chip.

Guided TeraHz waves are a hybrid of RF and optical signaling, using transmission of frequencies around 1012 Hz. These are propagated through microstripline waveguides possibly built with Cu and low-k or SiO_2. This approach is very attractive because it provides the opportunity to significantly extend the bandwidth of interconnect systems without having to change the material set. This technology may lend itself to smaller feature sizes than optical or RF and may be usable in “intermediate” interconnect layers.

More radical alternatives for global interconnect solutions include such areas as nanotube interconnects, spin coupling, and molecular interconnects. These options are in their early stages of development, and have a common critical need for total system concepts that demonstrate their utility in the interconnect function as well as manufacturing methodologies for their fabrication. Although many important features of radical solutions to the interconnect problem have been realized, additional creative approaches are needed that will provide the defined roadmap capabilities and meet the difficult challenges of cost and manufacturability.

In the case of more advanced interconnect options, the needs are to define and develop the technology, to define the total interconnect system parameters and approach, and to specify the needs from each component to meet the total interconnect system performance goals. For example, in the case of optical interconnects, it is easy to assume that this solution will meet speed requirements because the signal travels at “the speed of light”. However, to define the total interconnect system for this approach, it is necessary to consider the delays associated with rise and fall times of optical emitters and detectors, the speed of light and losses in the optical waveguides (if used), the signal noise due to coupling between waveguides, and a myriad of other details of this approach.

The global interconnect problem is currently being targeted by the MARCO interconnect focus center with both optical and 3D solutions. While these solutions have potential, only a limited number of optical approaches or 3D processes are being considered. Proposals for solutions where other funding sources already have investments will need to be carefully coordinated with the MARCO programs to both avoid duplication and leverage learning. In addition to optical or 3D solutions, other equally attractive novel

solutions, such as microwave interconnects, require further evaluation. Concepts for both wireless clock and high bandwidth multiplexed transmission lines have been previously funded by the SRC. These solutions can be die, package or hybrid die/package solutions.

Examples of novel solutions, new concepts or radical approaches to interconnect that are of interest to BEP are outlined below. This is just an example list; it is not intended to be inclusive.

- 3D wafer integration, specifically novel approaches to 3D that might exploit or extend capabilities for thinning and bonding wafers and capabilities for patterning, etching, aligning and filling dense, narrow inter-chip vias.
- Methods and technologies to build “transistor” grade electronic materials as a part of the interconnects at low temperature; where active devices are to be built within the interconnects.
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- Optical interconnects that deliver high bandwidth at low cost. Wavelength division multiplexing, on-die modulators, receivers and sources need system level feasibility assessment and prototype demonstrations, which are scalable.
- A high efficiency, high switching rate laser source, monolithically integratable into Si CMOS (at low cost), needs to be developed.
- A low power modulator, monolithically integratable into Si CMOS (at low cost), to be used in conjunction with an off-chip continuous laser
- Low power, high efficiency, small size optical detectors monolithically integratable into Si CMOS (at low cost)
- High efficiency TeraHz sources capable of monolithic integration into Si CMOS (at low cost)
- Low power TeraHz modulator that can be monolithically integrated into Si CMOS (at low cost)
- Low power, monolithically integratable into Si, CMOS (at low cost) TeraHz detectors of small feature size need to be developed. (The “small” detectors that are currently available are largely bolometric, and do not afford the bandwidth promised by the TeraHz carrier.)
- Thermal management capability compatible with high heat load of 3D or conventional interconnect
- Advanced low cost methods for heat extraction including liquid cooling, thermo-electric cooling or other novel solutions.
- Nanotube conductors
- Novel RF components (high Q resonators, inductors, capacitors, MEMS, etc)
- Cross Disciplinary solutions (BEP/Packaging, BEP/Design)
- Radical new alternatives to BEP issues