

# **Research in Support of Convergence of On-Chip and On-Package Interconnect**

## ***Introduction***

As the microelectronics industry moves along the technology treadmill, as indicated by the ITRS, both the die and the package performance advances. The minimum feature size on the die decreases, the die clock frequency/bus frequency increases, and the power increases. The required package is increasingly complicated in terms of number of pins, frequency response, and thermo-mechanical stability. Many of the issues concerning the die (and in particular its back-end) also concern the package. Indeed, the interface and the interaction between the die back-end and the package has become a new area of focus due to the impact of the package on the total die/package sub-system performance as well as mechanical integrity and the need to reflect this impact in the package design. The thermo-mechanical integrity issue of this subsystem has been recently highlighted with the introduction of mechanically weak low k dielectrics in the die backend. The appearance of wafer level packaging thick layers on top of passivation is another case in point.

The objective of this document is to discuss issues which are relevant to the die-package as a subsystem. It aims to foster design, analysis, and measurement methodologies and tools that address the on-chip and on-package electrical interconnect, heat transport, and mechanical reliability as features of an integrated subsystem. Issues which are pertinent only to the die or only to the package have been addressed in other "Needs" documents. By eliminating unduly specialized work on either chip or package in isolation in favor of approaches that optimize the chip-package subsystem as a whole, redundant effort can be minimized and device performance can be optimized.

This document does not claim to be comprehensive in its scope. By bringing up the new focus, it hopes to bring about new thinking which could lead to new research areas and new concepts.

## **1. Electrical issues**

### **a. Electromagnetic Modeling and Simulations.**

Tools that solve Maxwell's equations have routinely been used to analyze and create RLC-based models for package and board level interconnections. As chip performance increases, on-chip interconnections require more sophisticated RC and RLC (or equivalent) models that can use some of the same types of solutions of Maxwell's equations as those appropriate for package and board level interconnections. Thus, appropriately designed tools for solving Maxwell's equations can and should be applicable to both the die back-end and the package interconnect space. Viewed in this way, much work done concerning the die back-end can be leveraged for the package and vice-versa. Thus a focus on the die/package subsystem could reduce some redundancy work. With a single field solver for the die-package subsystem, the inherent dividing interface between die and package built into the previously separate design tools will be removed and a higher level of optimization could conceivably be obtained for the subsystem.

### **b. Global Signals/Signal Integrity.**

The same conditions as in item 1a apply here. Signal paths, both in the package and as on-die redistribution, along with the discontinuities due to vias, bumps, balls, and tortuous return paths need to be considered from the transistors outward. Handling these at the same time using the same tool might be more efficient than handling them separately and would resolve issues of potentially incompatible descriptions and tools.

### **c. Power delivery (high power/high performance chips)**

Approximately every 18-24 months, microprocessor frequencies double. At the same time there is an overall trend to higher current and lower voltages. These factors are producing a rapid increase in the di/dt generated noise in the chip/package sub-system, while at the same time acceptable noise margins are decreasing. This increasing impact of di/dt generated noise is seen at all levels of the power loop, from chip to package to motherboard to the voltage regulator module. This creates a critical need for improvements in technology to reduce or circumvent di/dt generated problems at all system levels.

Whereas more work on-die (such as circuit control techniques and architectural changes to limit the di/dt without sacrificing thermal demands, as well as on-chip decoupling capacitance) and on package (low inductance and low resistance, small form factor decoupling capacitor technologies) are being conducted separately, a die-package subsystem approach to deal with the power delivery issue could lead to better performance and trade-offs and lower cost.

#### **d. Clock distribution (high frequencies)**

Increasing clock frequencies exacerbate skew and jitter problems. A die-package subsystem design approach will help alleviate them and is worthy of analysis. In addition, from a subsystem perspective, clock distribution might be better optimized through a reevaluation of the present on-die network. Recent research in RF clock distribution is such an example.

### **2. Thermo-mechanical issues**

#### **a. Materials**

A myriad of new materials are being considered to provide the requirements of smaller, higher performance packages for advanced ICs. Many of the same requirements are being faced by researchers focused on the die back end. These trends point to a need for convergence of materials studies for both areas. Indeed, the issues and the controlling material properties and mechanics are the same, while their actual numerical values may be different: interface materials interaction including die-package material interface properties, thermo-mechanical integrity (especially of new low k materials), stress-strain characteristics, delamination, and CTE, are some examples.

Key area of research focus should be an understanding of material property variation as a function of processing and local stresses. Characterization of reliability by dynamical thermal and mechanical stresses (such as micro-defects, debonding between materials, microstructures) is critical. Specifically, for new package dielectrics, dielectric strength and metal migration, adhesion and surface roughness, aging properties, are examples of studies, which have also been areas of research for die back end materials. Overall, materials reliability, whether for die back end or for packages, would benefit from a common set of modeling and experimental tools and methodologies that allow for efficient validation and predictability.

#### **b. Thermal management**

Heat generation is a major issue in advanced high performance ICs, and is expected to become even more critical as performance increases and environments become more demanding. With the decreasing heat conductivity of low k dielectrics anticipated in future generations of ICs, the impact of interconnect selfheating and possible degradation is an increasingly important consideration. With the trend to high current, low voltage, IC processes can result in situations where heat generation in the package must also be considered. The standard approach of separate die and package thermal solutions is no longer appropriate. Solutions for heat extraction are very much a complete die-package system design issue (power density, hot spots, attach materials, heat spreaders, air flows, acoustics, volume constraints, etc.). Note that whether cooling is done through the board or away from the board, thermal loading and proximity effects for the entire board or system must be considered.

Overall, a die-package subsystem approach to thermal management potentially could unveil new optimal solutions.

#### **c. Modeling**

Many modeling and simulation issues are generic for chip and package, with only the geometry and the numerical values of the properties changed. The specific chip-package interface, solder balls, die attach, etc., have traditionally been handled by the package designers. But with the chip backend becoming weaker with low-k dielectrics, thermal and mechanical package deformations impose more significant displacements on the chip. The chip-package, and in some cases the chip-package-board, system needs to be considered as a whole. Predictive tools are essential that allow us to evaluate the robustness of the chip - package-board and that point to locations of potential reliability failure where robustness must be increased. Approaches in need of improvement include multiscale modeling, transfer of geometry among fabrication, electrical, and mechanical ECAD tools, and, a standardized and practical treatment of interface reliability.

### **3. Metrology**

Measurements of the electrical and mechanical behavior of the chip, of the package, and of the chip-package interconnects, including die-attach, solder, adhesive, etc. are commonly utilized to provide accurate input data for modeling and simulation, and to verify that the design performance is achieved in the released product. Designs with the new subsystem concept may require new measurements.

a. *Electrical*. If the package is to be capable of offloading some of the signal interconnections from the chip, the package must have adequate electrical performance at frequencies higher than currently utilized in packages. This performance will require verification, and eventually, prediction.

b. *Thermo-mechanical*. The issue here is new on-chip interconnect materials, such as

copper-low k, and new chip-package interconnect system designs that may put new sets of mechanical stresses on both the chip and the package and may impact overall reliability. Measurements are needed to provide the appropriate material properties and to verify that the modeling has accounted for actual boundary conditions and failure modes. Many of these measurements are at the outer boundary of current capability.

#### **4. Advanced Solutions**

Consideration of the chip and package as an integrated system opens up the possibilities for advanced solutions to the issues addressed by traditional interconnect and packaging designs. These include, for example:

- a. Optimized partitioning of interconnect systems in conjunction with, for example, very fine-pitch die-package connections, with multiplexed IO signals at very fast rate, with digital modulation technique in which a bit stream is serialized and then phase modulated,
- b. Optical interconnects for intra-chip and inter-chip communications through the package. In this scheme, alignment of sources/receivers with the interconnects is an important issue.
- c. Wireless interconnect schemes to eliminate wire bonding, solder balls, conductive adhesive, or other direct electrical connections. As an example, with the clock frequencies increasing, wireless local interconnect schemes have been proposed and researched. Such an approach would require a die-package subsystem focus.
- d. Three dimensional schemes: here the partition between die and package is blurred. A subsystem approach is desired.
- e. Out of the box sub-system concepts. There are potentially new concepts of die-package subsystems to be envisioned. A hope of this document is to stimulate such ideas.

#### ***Conclusions***

With ever more advancing chips, there is a trend toward convergence of the die back end and the package. This document attempts to bring this convergence into focus and discuss some examples of needed work with the goal of stimulating further thinking and, potentially, unveiling new areas of research leading to novel solutions.