

Packaging Thrust Strategic Needs

Introduction

The purpose of this document is to define the needs of the SRC member companies in the area of Packaging, and to highlight specific areas where the SRC program will focus. In a proposal selection process, consideration will be given to the facilities required for research in specific areas, the compatibility of problems with the university environment and time scale, and the work being done in industry and at other consortia. In this document Packaging is defined to include all of the processing and materials associated with providing the interface between the chip and the macroscopic world. In some cases, such as global interconnect, some aspects of Packaging research will need to include the interaction between the package and the on-chip interconnect system. Of particular interest are novel package design and packaging processes to improve the performance of this interface.

Background

The 2003 edition of the Internal Technology Roadmap for Semiconductors (ITRS) identifies grand challenges and difficult challenges facing the Assembly and Packaging area. These challenges consist of multiple needs and issues as compiled by the International Technology Working Group (ITWG) of the ITRS. These challenges are classified as either near term (out to 2009) or as long term (2010 and beyond). This Strategic Needs document serves to identify critical areas where new capability is needed, and to prioritize and direct the investment in university research.

Grand challenges that can be impacted by the Packaging Thrust are seen not only in the ITRS focus area of Assembly and Packaging, but also in Interconnect; in the crosscut of Environment, Safety and Health; in the crosscut of Modeling and Simulation and in one of the ITRS special topics, Wireless Technology. The Pkg Thrust has currently organized into four sub-thrusts. Some of these sub-thrusts are linked with the Back End Processing Thrust (BEP) of the IPS or with other Science Areas within the Semiconductor Research Corporation (SRC). The sub-thrusts of the Pkg Thrust are Global Interconnect Systems, Thermal Solutions, Materials and Interfaces, and New Packaging Concepts. Significant efforts are also present in the cross thrust areas of Reliability and Copper Low k. In this document we will first describe the most significant challenges from the ITRS Working Groups that are recommended for IPS university support. We will then describe additional challenges specific to the current Pkg sub-thrusts.

Grand Challenges – International Technology Working Groups

Assembly and Packaging Working Group

Tool and methodologies are needed to address chip and package co-design.

Assembly and packaging have significant effects on the operating frequency, power consumption, form factor, reliability, and cost of the final products. To meet the stringent design, cost, performance, cycle time, environmental and regulatory requirements for such products, concurrent chip and package design is required. Simulation tools and modeling methodologies are needed that simultaneously address all critical features of the final structure, including mechanical, electrical, and thermal performance. Research interests include simulation tools,

modeling methodology, new materials development and assessment of materials for electrical and mechanical performance and environmental impact. This need is most acute in RF and mixed signal applications where inductance, capacitance and parasitic values associated with interconnect, substrate and packaging are important design parameters affecting both the bandwidth and signal integrity. Work in this area needs to comprehend the possible both ability to assess cost impact of design options and potential commercialization of research results by vendors from the electronic design automation (EDA) community.

Interconnect Working Group

New materials are needed & manufacturable interconnect structures must be engineered.

Low dielectric constant (low k) materials and low resistivity metals are needed to minimize interconnect delays. In addition to meeting the electrical requirements of future devices, these materials and structures must meet mechanical requirements compatible with chemical mechanical planarization (CMP), etching, wirebond processing, and other assembly and packaging processes. The ITRS notes that mechanical damage by CMP and packaging stresses has significantly retarded the implementation of low k material. Cu/low k systems need predictive models and failure detection metrology that will assess the compatibility of these structures with assembly and packaged device use stresses. In addition to meeting construction and manufacturing challenges, tools are needed that will facilitate design optimization.

Modeling and Simulation Working Group

Need 5-40 GHz models and simulation capability and models for newly introduced materials.

New simulation techniques that are both more comprehensive and computationally efficient are required for high frequency packages and packaging materials applicable to RF, analog, digital and mixed signal circuits. These simulators must be capable of handling new complex, real world models and simulate in either 2D or 3D mode while considering inherent statistical variations. Multi-layer dielectrics, overmold and substrate dielectric effects, power and ground inductances, cross talk, substrate return paths, substrate coupling, EM radiation and heating effects must all be considered. Applications at higher frequencies must consider the global effects that become more pronounced at the higher frequencies. Simulating third harmonic distortion for 40 GHz applications means modeling harmonics up to 120 GHz. Models and simulators must make more effective and efficient use of the computing resource. New materials are required for all aspects of high frequency packaging and interconnect systems. Present materials are facing physical limitations that prevent further scaling. Equipment, process, device and circuit models must include these new materials. But the models themselves must be extended to better describe the material properties and the operating environment to which the materials are to subject. Real world models must include cost, process, manufacturing, reliability, etc. indicators to reduce experimental effort and costs associated with an over-reliance on hard prototypes.

Wireless Technology Working Group

Need tools capable of referencing layout, material properties, etc. to simulate what-if scenarios.

Wireless applications are one of the chief drivers for semiconductor technologies and products. The success of these systems is dependent on meeting the simultaneous constraints of costs, time-to-market and customer specified performance. The complexity and high costs of implementing System-on-a-Chip (SOC) applications have caused a near term shift in focus to

System-in-a-Package (SiP) applications. While the costs may be more modest, the system's complexity remains the same. Comprehensive design tools that assist in design decision process do not exist. Packaging design decisions such as size, number of layers, materials or technology are made based on experience or through design iterations. Design compromises are forced due to competing and conflicting requirements. Circuit layout, package pin assignments and layout, packaging and package material choices all affect RF performance. Tools are needed that can properly simulate the operation of a typical RF circuit in a package or module or additionally, compute the effects of the package and packaging materials above the elemental model level.

Difficult Challenges – Packaging Sub-thrusts

The following sections describe some specific needs within the current Packaging sub-thrusts.

Overall Issues

The ITRS identifies a number of overall packaging issues. These items affect all sub-thrusts. Technology must respond to rapidly changing, complex business requirements. Customers have increased expectations for faster delivery of new and volume ready products. There is a need for improved integration of the entire product design and manufacturing process. The emphasis is for faster design cycles, faster first prototypes and faster ramps to volume production. Increased purity requirements for process and materials together with an increasing number of processing steps coupled with process and product complexity require managing the increased complexity while keeping costs in check. There are increasing global restrictions based on environmental issues. This means regulations and technology restrictions in different countries and geographical areas must be met. Technologists must comprehend items such as Pb-free and other chemical/material restrictions, and tighter EHS/Code requirements in the face of the need for new materials to be introduced into packaging and interconnection systems.

Global Interconnect Systems

Traditional interconnect and scaling techniques will no longer meet the performance requirements for high frequency global interconnects. Material innovation, accelerated design techniques, and unconventional combinations of packaging and on-chip interconnect are required to find acceptable solutions beyond today's copper and low k metallization for packages and ICs. Basic questions remain in methods of stacking die, passive component integration, the use of new technologies such as optical and microwave interconnect, and interconnect shielding.

New packaging materials, structures and assembly processes will be needed to handle the high frequency, power, and operating environment requirements of global interconnect for future devices. New solutions will be required to counter the increased thermal and mechanical problems associated with assembly and packaging of complex materials and structures used to fabricate new on-chip global interconnect structures. Modeling, detection, testing and control of thermal and mechanical failure mechanism will be a key need.

Materials and Interfaces

Various industry consortia are actively pursuing process definition and materials selection for Pb-free assembly in an effort to comply with the EU directive for Reduction of Hazardous Substances (RoHS). Several Pb-free solder alloys are being considered for industry use, all with compositions near the SnAgCu ternary eutectic. There are no Pb-free solder alternatives with

liquidus temperatures above 240°C and lower than 280°C. With such a gap in melting point temperatures there is no room for solder hierarchy on organic substrates when using Pb-free processing. Further, the long-term reliability performance of these candidate SnAgCu solder compositions in electronic assemblies is largely unknown. While SnAgCu solder connections are now routinely being tested using the generally accepted accelerated reliability tests for SnPb solder joints, little fundamental basis exists for extrapolating these accelerated test conditions to field reliability performance of SnAgCu solder joints. Differences in SnAgCu fatigue mechanisms and micro-structural interactions may very well require different reliability extrapolation methodologies than have been previously developed for SnPb solder.

Establishing the fundamental knowledge basis for SnAgCu reliability is expected to require additional research in the thermal fatigue and deformation behavior of these alloys along with a clear understanding of the micro-structural stability of SnAgCu solder joints in combination with various components and card surface finishes. Further complicating the SnAgCu reliability question is the case of mixed solder alloy assembly, which is expected to occur during the industry transition from SnPb assembly to SnAgCu assembly.

The SRC Packaging TAB has long emphasized the criticality of interfacial integrity in package performance and reliability. SRC support of scientific studies in this arena over many years has produced significant strides in scientific understanding and improvement of package interfaces. The introduction of higher process temperatures for Pb-free assembly, however, has further elevated the physical demands on package interfaces and materials. Consequently studies investigating techniques and materials that increase package robustness through process temperatures at and beyond 260°C will be of interest.

New Packaging Concepts

Radical new packaging concepts are needed to allow packaging costs to follow the die cost reduction curve. Previously, packaging margins were inadequate to justify large research investments. Packaging costs are now a substantial portion of the total device costs. Substrate costs are the most significant barrier to the wide spread implementation of Flip Chip technology today. Advanced devices and/or their operating environments have exceeded the parameters of today's packaging technology. There is the need to close the gaps between the substrate technology and the chip technology. Witness the difference in the minimum chip pad pitch capability and the minimum substrate pad pitch capability.

Material innovation, accelerated design, packaging and unconventional interconnect are needed to address the global wiring scaling issues. Improved organic and ceramic substrate materials are needed to increase wireability and core via density at low cost. Higher frequency applications will require greater impedance control and lower dielectric loss. A combination of high k and low k materials are needed to allow for the low cost embedding of passive components into the substrate. The substrate materials will need to dissipate increasing amounts of heat generated by high power applications and higher frequency applications. Novel new processes, structures, and interconnect are required for the next generation of devices. Smaller gaps and higher bump density will necessitate improved underfills for flip chip type technologies. Any new packaging technology must seamlessly handle thinned die, stacked die, large and small

die, and the integration of passive components either embedded or discrete. Wafer level packaging capabilities are needed.

Biological, organic and nanostructure devices will require new packaging concepts and technologies. Novel package-chip systems concepts are needed to incorporate optical and electronic systems into a single cost-effective component. Models and physical design tools are needed for integration of such optical/electronic systems. The rapid introduction of new materials and processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity will create integration and material characterization challenges. Radical solutions to provide higher wiring density to support greater than 20 lines per mm and higher bump densities are needed along with processes and production techniques that are less discrete and are more wafer-like. The current desired operating environment, density, and operating temperature for high pad count small die, high power density and high frequency die exceed the capabilities of current assembly and packaging technology. Tighter tolerance and three-dimensional control of the interconnect features are required to achieve necessary circuit performance and reliability.

A new bump-less area array technology is needed. New bump and underfill technologies are needed to assure low k dielectric integrity. Material challenges abound in finding materials that will meet the needs for high conductivity, low permittivity, lower costs, manufacturability and environmentally friendly. New techniques must present cost efficiencies that are better aligned with silicon wafer processing. The need for increased wireability, lower dielectric loss, improved impedance control and embedded passives all at low cost are a considerable challenge.

Thermal Solutions

High frequency die, high power die, small die with high pad count and increased operating temperatures may exceed the thermal capabilities of current packaging technology. The ITRS has said, "Hot spot thermal management needs to be addressed before 2007." They have identified a thermal brick wall at 5-micron lines and spaces and the need for an upper bound on the thermal management capability of future packages.

Thermal management must consider the use of low k, high k, increased via density and the increased density of Cu and other material interconnect that utilize thin line widths. Flip chip, the use of underfills and heat slugs further couple the device to the substrate and increase thermal coupling between parts. Thermal modeling must include the effects of thin die, stacked die, very large and very small die, etc. Once assembled, the packages must meet Moisture Sensitivity Level (MSL), Temperature Cycle (T/C) and other reliability and Accelerated Life Tests (ALT). Coordinated design tools that integrate simulators into the design environment are needed address the issue of chip, substrate and package co-design. Such a design environment would include tools for transient thermal analysis and simultaneous thermal, electrical, and mechanical analysis.

Conclusion

This "Needs" document is not intended to be inclusive, but rather to identify some of the Packaging areas currently identified as in need of concentrated research. Other areas of needed

research exist, and may be described later as needs change or updated information becomes available.