2005 Packaging Thrust Strategic Needs

The following sections describe some specific needs within the current Packaging sub-thrusts.

Overall Issues

The ITRS identifies a number of overall packaging issues. These items affect all sub-thrusts. Technology must respond to rapidly changing, complex business requirements. Customers have increased expectations for faster delivery of new and volume ready products. There is a need for improved integration of the entire product design and manufacturing process. The emphasis is for faster design cycles, faster first prototypes and faster ramps to volume production. Increased purity requirements for process and materials together with an increasing number of processing steps coupled with process and product complexity require managing the increased complexity while keeping costs in check. There are increasing global restrictions based on environmental issues. This means regulations and technology restrictions in different countries and geographical areas must be met. Technologists must be cognizant of environmental requirements and demands, as Pb-free, halogen-free, and other chemical/material restrictions become institutionalized, and design for materials reclamation factors in to product considerations for new packaging and interconnection systems.

Global Interconnect Systems

Traditional interconnect and scaling techniques will no longer meet the performance requirements for high frequency global interconnects. Material innovation, accelerated design techniques, and unconventional combinations of packaging and on-chip interconnect are required to find acceptable solutions beyond today's copper and low κ metallization for packages and ICs. Basic questions on scalability, performance envelopes, and manufacturability remain in methods of stacking die, passive component integration, the use of new technologies such as optical and microwave interconnect, and interconnect shielding. Viable modeling and validation tools that will help quantify technology envelopes continue to be essential to help designers and technologists make robust decisions and trade-offs for technology selection

New packaging materials, structures and assembly processes will be needed to handle the high frequency, power, and operating environment requirements of global interconnect for future devices. New solutions will be required to counter the increased thermal and mechanical problems associated with assembly and packaging of complex materials and structures used to fabricate new on-chip global interconnect structures. Modeling, detection, testing and control of thermal and mechanical failure mechanisms will be a key need.

Materials and Interfaces

As Pb-free and RoHS compliance (EU directive for Reduction of Hazardous Substances) becomes industry standard, new packaging materials and systems must assure compatibility. This is expected to increasingly become a development rather than research focus for member companies. Knowledge of differences in SnAgCu fatigue mechanisms and micro-structural interactions will need to be embedded into increasingly complex reliability models to assure materials and interface integrity. Another key challenge in the Pb-free arena will be developing

solder and other packaging materials that enable low temperature processing. This is expected to be a key area of interest in the future to expand process windows.

As materials and interfaces are addressed, the ability to meet wireless (RF) requirements for some applications will be needed. Verification that new materials will not adversely suppress RF signals and whether or not increased crosstalk in 3D packaging will impact signal integrity are examples of material considerations that must be addressed.

Challenges from the thermal thrust will drive new materials challenges, in particular an understanding of thermal interfaces and the associated semi-structural integrity that new applications may require for these materials. In particular, as cost is reduced and thermal performance in increased, ultra-thin bond lines (film thicknesses) of thermal interface materials may be required, potentially bearing some measure of the structural load of the package.

New packaging concepts and innovative global interconnect solutions, each discussed under separate sections here, will both drive new materials and interface challenges. As the backend process and structures take on ever more fragile dielectrics, and backend dimensions drive more intimate package/chip interfaces, chip-package mechanical interaction concerns will need to be addressed. It is envisioned that new classes of materials, including nano-structures and bio-structures, will offer potential solutions. With ever increasing complexity of the chip-package communication pathway, materials and interfaces based on self-assembly and self-healing / auto-repair need to be considered.

New Packaging Concepts

Radical new packaging concepts are needed to allow packaging costs to follow the die cost reduction curve. Previously, packaging margins were inadequate to justify large research investments. Packaging costs are now a substantial portion of the total device costs. Substrate costs are the most significant barrier to the wide spread implementation of Flip Chip technology today. Advanced devices and/or their operating environments have exceeded the parameters of today's packaging technology. There is the need to close the gaps between the substrate technology and the chip technology. Witness the difference in the minimum chip pad pitch capability and the minimum substrate pad pitch capability.

Material innovation, accelerated design, packaging and unconventional interconnect are needed to address the global wiring scaling issues. Improved organic and ceramic substrate materials are needed to increase wireability and core via density at low cost. Higher frequency applications will require greater impedance control and lower dielectric loss. A combination of high κ and low κ materials are needed to allow for the low cost embedding of passive components into the substrate. The substrate materials will need to dissipate increasing amounts of heat generated by high power applications and higher frequency applications. Novel new processes, structures, and interconnect are required for the next generation of devices. Smaller gaps and higher bump density will necessitate improved underfills for flip chip type technologies. Any new packaging technology must seamlessly handle thinned die, stacked die, large and small die, and the integration of passive components either embedded or discrete. Wafer level packaging capabilities are needed.

Biological, organic and nanostructure devices will require new packaging concepts and technologies. Novel package-chip systems concepts are needed to incorporate optical and electronic systems into a single cost-effective component. Models and physical design tools are needed for integration of such optical/electronic systems. The rapid introduction of new materials and processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity will create integration and material characterization challenges. Radical solutions to provide higher wiring density to support greater than 20 lines per mm and higher bump densities are needed along with processes and production techniques that are less discrete and are more wafer-like. The current desired operating environment, density, operating temperature for high pad count small die, high power density and high frequency die exceed the capabilities of current assembly and packaging technology. Tighter tolerance and three-dimensional control of the interconnect features are required to achieve necessary circuit performance and reliability.

A new bump-less area array technology is needed. New bump and underfill technologies are needed to assure low κ dielectric integrity. Material challenges abound in finding materials that will meet the needs for high conductivity, low permittivity, lower costs, manufacturability and environmental friendliness. New techniques must present cost efficiencies that are better aligned with silicon wafer processing. The need for increased wireability, lower dielectric loss, improved impedance control and embedded passives all at low cost is a considerable challenge.

For any new packaging technology, the impact of systems under normal use conditions on package reliability and the impact of the package on the device reliability have to be investigated thoroughly for the robust device-package-system integrity and optimization. In addition to the above challenges, the major issue is the validation of thermal/mechanical models on reliability of device/package/system combination. This validation may be accomplished by the embedded temperature and stress sensors in device and/or package substrate. Studies related to the sensors and the feasibility of the combined structures are also needed.

In general there is interest in understanding the in-situ evolution of material properties, stresses, temperature and structural integrity. Research is needed in how these may be sensed, measured and interpreted to provide meaningful inputs for predictive performance and reliability modeling and validation.

Thermal Solutions

Among the primary beneficiaries of advanced wafer fab technologies are microprocessors. Present microprocessor designs split the device into core logic and cache memory areas. As much as 90% of power usage occurs in the core logic area, which may be only 25-50% of the total die area. The heat flux today reaches 250-300 W/cm^2 in these core logic areas. Extrapolating to future fab technology suggests that management of heat flux on the order of 500-1000 W/cm^2 will be necessary. To date thermal management of such devices has relied on the use of ever-larger heatsinks and attached fans. With processors being used in products with continuingly reduced volumes (small form factor computers, thin and light notebooks, blade servers) there is a need for new thermal management solutions with greater volume efficiency (W/cm^3) than present solutions. The same need also arises for devices with lower heat flux (<100

W/cm^2) that are used in extremely small, portable devices such as PDAs or advanced telephony devices that cannot accommodate high cost solutions. Such applications may also require System in Package designs (including stacked die and/or packages) resulting in new needs for unique thermal solutions.

Thermal management solutions must account for the use of low κ insulators on the die and increased interconnect density on-chip and chip-to-package, and decreased interconnect geometries. These new materials and geometries increase the sensitivity of the packaged devices to mechanical and thermo-mechanical stress. No reduction in reliability requirements is anticipated, and in some cases, increased reliability requirements to accept extreme conditions (corrosive ambients, high temperatures >150°C, etc) may be required.

Package thermal resistance (Θjc) for the high power processors is typically <0.50 °C/W. Standard measurement techniques depending on thermocouples or thermistors for measurement of reference temperatures are not sufficiently accurate for determination of thermal resistances below this level. Measurement of temperature distributions on die is also not sufficiently spatially accurate given that hotspot regions may be as small as a few microns square. New techniques for in-situ measurements on functional die are necessary for comparison to data generated using thermal test devices.

Coordinated design tools that integrate simulators into the design environment need to address the issue of chip, substrate and package co-design. Such a design environment must include tools for simultaneous thermal, electrical, and mechanical analysis.

Conclusion

This "Needs" document is not intended to be inclusive, but rather to identify some of the Packaging areas currently identified as in need of concentrated research. Other areas of needed research exist, and may be described later as needs change or updated information becomes available. Primary thrusts continue in the realm of global interconnect, materials and interfaces, thermal management, and truly novel new packaging concepts.