Back End Processing Research Needs Statement

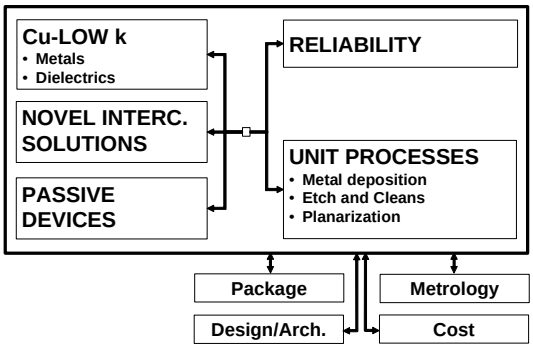
This document summarizes the research needs of the SRC member companies in the area of Back End Processes (BEP). For additional background and definitions, please refer to the ITRS Interconnect Roadmap (http://www.itrs.net/Links/2005ITRS/Interconnect2005.pdf).

I. INTRODUCTION

The BEP areas of interest can be grouped as follows:

- Cu-low k extendibility: evolutionary solutions.
  - Metal.
  - Dielectrics.
- Novel interconnect solutions: non-evolutionary alternatives that go beyond conventional metal/dielectric interconnects.
- Unit processes:
  - Metal deposition.
  - Etch and cleans.
  - Planarization.
- Reliability (electrical and mechanical).
- Passive devices: materials for passive devices within the interconnect structure.

The interrelation between these five areas is shown in the figure below: Cu-low k, Novel Interconnect solutions and Passive devices define the stack and the needs; Unit processes refers to the modules that make them possible; and Reliability is an overall requirement. In addition, package, cost, design and architecture considerations, and metrology play an important role in interconnect decisions.



II. RESEARCH NEEDS

In this section, the core needs for which research is needed (experimental, simulations or theoretical) are enumerated.

II-1. CU-LOW K EXTENSIBILITY RESEARCH NEEDS

II-1a. Metals

- Decrease of the resistivity of narrow lines (< 30 nm line width) by optimizing the microstructure (grain size, texture), decreasing interface roughness, or by any other means.
- Alternate metal/barrier combinations with lower effective resistivity than Cu at small dimensions (< 30 nm line width).
- Fundamental limits of metal-based interconnects from a performance (conductivity) and reliability (electromigration and stress voiding) perspectives.
- Methods to reduce the resistance of contact/silicide and contact/gate metallization.

II-1b. Dielectrics

- Low-k low-porosity dielectrics, including SiCOH, polymers and other classes of materials. Performance is related to the following considerations:
  - Electrical: relative permittivity (k) below 2.3, low leakage, high breakdown voltage.
  - Porosity: non-porous or low porosity materials are preferred for integration ease.
  - Mechanical integrity: acceptable fracture toughness, residual stresses, elastic modulus, interface adhesion, thermal expansion coefficient.
- Barriers: refer to the “Metal deposition” section (II-1b).
- Porosity related topics:
  - Pore sealing techniques compatible with dual damascene patterning and ALD barriers, with minimal impact to the effective stack permittivity.
  - Measurement of size, distribution and connectivity of pores in low-k dielectrics.
- Damage during etch and cleans: refer to the “Etch and cleans” section (II-2b).
- Design of novel dielectrics to optimize k and elastic modulus from first principles.
- Air-gap approaches.

II-2. UNIT PROCESSES RESEARCH NEEDS

II-2a. Metal deposition

- Gap fill for 10:1 aspect ratios for line widths below 30 nm, with minimal overhang.
- Barrier and seed layers: thin (< 3 nm), conductive, conformal, smooth (to ameliorate electron scattering) and “electroplatable” barrier/seed layers. Barrierless ILDs.
- Novel techniques to fill lines and vias, including electroless plating, plating on ultra-thin seed layers, CVD, or other techniques.
- Void detection in copper lines.

II-2b. Etch and cleans

- Wet chemical fundamentals: removal of resist, anti-reflecting coatings and post etch polymers without degradation of the dielectric or interfaces.
- Dry etch selectivity: integrity of 193 nm resists during dielectric etch.
- Damage during etch and cleans of low k dielectrics:
  - Technique to repair damage created during etch and cleans.
  - Metrology to measure sidewall dielectric damage and residues with < 2 nm resolution.
- Fundamental understanding of plasma-surface interactions for etch and cleans of low k materials with k < 2.3.
- Surface preparation and cleaning techniques beyond wet and plasma cleaning, such as supercritical fluids, cryogenic aerosols, and laser cleaning.

II-2c. Planarization

- CMP of weak (porous or polymer) dielectrics:
  - Methods to decrease the mechanical loading during barrier removal.
  - Comprehensive understanding, including chemical, mechanical, fluid and tribological aspects to define pad, slurry and process conditions.
- Alternative metal/dielectric planarization techniques such as Chemically Enhanced Planarization, Electropolishing, and Electro-chemical-mechanical polishing for improved feature control and low stress compatibility with weak dielectrics.

II-3. RELIABILITY RESEARCH NEEDS

- Electromigration (EM):
  - Performance of vias with non-hermetic barriers at the bottom.
  - Reliability of realistic interconnect trees.
  - Methods to improve electromigration and stress voiding resistance with minimum impact to interconnect resistance.
- Electrical reliability of low k dielectrics (porous and non-porous) and thin barriers, including breakdown voltage and Cu migration.

- New experimental methods to assess the mechanical integrity of stacks with multiple interconnect layers.
- Understanding of the requirements of Cu-low k stacks for meeting mechanical integrity requirements that comprehends elastic constants, fracture toughness, thermal expansion coefficient, adhesion energies, defects, and for porous dielectrics, porosity (pore size, shape, aspect ratio and connectivity).

II-4. NOVEL INTERCONNECT SOLUTIONS

II-4a. 3D Integration (wafer-to-wafer, die-to-die, die-to-wafer)

- Novel approaches to enable high throughput deep sub-micron alignment and bonding, such as self-alignment concepts
- Low temperature bonding (below 300 ^{o}C):
  - Conductive materials to enable low temperature, low pressure bonding.
  - Novel bonding-enabling surface treatments and SAM layers.

II-4b. Optical interconnects

- On-die modulators capable of: bandwidths greater than 30 Gb/s at 1V or lower; insertion loss below 3 dB; input capacitance below 10 fF; area under 100 μm^2; operation at 100 ^{o}C; process below 450 ^{o}C; withstand 450 ^{o}C anneals:
  - Electro-optical materials with $\Delta n/n > 0.001$ at 1 V, compatible with Back End processing.
  - Fully integrated CMOS quantum confined stack effect modulators.
- Couplers to send light from and into the chip.
- Light sources:
  - High power (0.3-1 W) high efficiency laser-fiber/waveguide laser that can be integrated on the package or on the board.
  - Directly or indirectly modulated lasers.
- Materials to enable Back End compatible detectors to enable the following: Current per unit of output capacitance above > 100 mA/fF; Photo/dark current ratio above 10; Responsivity greater than 50 %; Bandwidth higher than 25 Gb/s at 1V or lower.

II-4c. Carbon nanotubes (CNTs)

- Contacts: methods to minimize contact resistance, selection of metal contacts.
- Growth of densely packed bundles with hundreds of metallic CNTs using catalysts.
- Functionalization and placement techniques.
- Metrology:
  - Statistically meaningful DC and high frequency characterization of individual SW, DW and MW CNTs, and of bundles of CNTs. Scaling of bundles of CNTs.
  - Wafer-level metrology to measure number and size (radius) of CNTs between contacts.
- Understanding of scattering phenomena.

II-5. PASSIVE DEVICES

- High permittivity materials (k > 20) for decoupling capacitors.
- Magnetic materials to reduce the area of inductors.
- Materials for thin film resistors.