Packaging Thrust Strategic Needs

Introduction

As silicon technology continues to evolve along Moore's Law, the challenges to current and future packaging technology have continued to increase. On the one hand, packaging technology must respond to the technically complex packaging demands of advanced silicon and systems that are seeing increased convergence of computing and communications; and rapidly changing, complex business requirements on the other. Besides providing environmental protection, packaging is a key enabler of interconnects scaling, power delivery & removal and high speed IO and it will continue to be challenged to evolve in these areas. Additionally, due to increased expectations for faster delivery of new and volume ready products, there is a need for improved integration of the entire product design and manufacturing process. The emphasis is for faster design cycles, faster first prototypes and faster ramps to volume production. Finally, packaging must continue to meet all relevant global restrictions based on environmental issues such as Pb-free and halogen-free material systems.

In this document we attempt to highlight some of the key strategic challenges facing packaging technology. It is extremely important to recognize that packaging is a key element of a complete computing/communications system and all the needs described in this document must be understood within the context of the system where the technology will be used. Some of these contextual elements include micro-architecture, design, and interactions of the compute/communication elements, application driven reliability requirements, form factor considerations and the business context that will dictate the cost the packaging technology

Global Interconnect Systems

It is generally understood that traditional interconnect and scaling techniques will no longer meet the bandwidth requirements for high frequency global interconnects and that non-conventional combinations of system boards, packaging and on-chip interconnect are required to find acceptable solutions beyond today's copper and low κ metallization for packages and ICs. However, basic questions on scalability, performance envelopes, and manufacturability are still unanswered in the most commonly cited non-conventional methods of interconnects scaling, including stacking die, optical and microwave interconnect. In addition, material innovation and comprehensive system level design techniques will be needed to enable non-conventional scaling.

Viable modeling and validation tools that will help quantify technology envelopes for both the conventional and non-conventional interconnect schemes, continue to be essential to help designers and technologists make robust decisions and trade-offs for technology selection. These tools must be both accurate and fast to handle the increasingly complex structures which must be analyzed to enable more design trade-off analyses. They must also allow assessment and prediction of system level electrical, thermal, and mechanical and reliability performance and optimization to assist designers in making the appropriate trade-offs.

One of the key limiters for faster computing and communication is the switching noise either due to DI/DT or due to coupling. As the number of cores and/or bus speeds are increased, the need for effective decoupling will be more and more imperative; therefore, efficient solutions for providing such massive decoupling in cost effective structures are imperative.

New solutions will be required to estimate and resolve the thermal and mechanical problems associated with assembly and packaging of complex materials and structures used to fabricate the global interconnect structures. Prediction of electrical performance and modeling, detection, testing and control of thermal and mechanical failure mechanisms will be key needs.

Materials and Interfaces

New packaging materials, structures and assembly processes will be needed to handle the high frequency, power, and operating environment requirements of global interconnect for future devices. These materials, structures and assembly processes, must be compliant with current and future environmental regulations (e.g. RoHS). Some areas of interest to SRC members are:

- Knowledge of Pb-free solder fatigue mechanisms and micro-structural interactions will need to be embedded into increasingly complex reliability models to assure materials and interface integrity. Another key challenge in the Pb-free arena will be developing solder and other packaging materials that enable low temperature processing to expand process windows and/or to enable packaging of low temperature capable devices.
- Challenges from the thermal thrust will drive new materials challenges, in particular an understanding of thermal interfaces and the associated structural integrity that new applications may require for these materials. In particular, as cost is reduced and thermal performance is increased, ultra-thin bond lines (film thicknesses) of thermal interface materials may be required, potentially bearing some measure of the structural load of the package.
- New packaging concepts and innovative global interconnect solutions, each discussed under separate sections here, will both drive new materials and interface challenges. As the backend processes and structures take on ever more fragile dielectrics, and backend dimensions drive more intimate package/chip interfaces, chip-package mechanical interaction concerns will need to be addressed. It is envisioned that new classes of materials, including nano-structures and bio-structures, will offer potential solutions. With the increasing complexity of the chip-package communication pathway, materials and interfaces based on self-assembly and self-healing / auto-repair need to be considered. Methods to improve the fracture toughness of package materials over a wide temperature range using nano-structures or other means are likely to be a fertile field for investigation.
- As the reliability of packages is partly driven by the reliability of interfaces, improved understanding of the fatigue properties of interfaces is desired. Interfaces of interest include polymers to oxides, polymers to metals, and oxides to metals or barrier layers. Both molecular and macroscopic level understanding of the fatigue behavior under various strain loading regimes is needed. Traditional test techniques to establish the reliability of interfaces are time consuming. In an era of parallel and shortened product development cycles, faster interfacial fatigue test methods are desired.
- Improved organic and ceramic substrate materials are needed to increase wireability and core via density at low cost. Higher frequency applications will require greater impedance control, lower dielectric loss and lower roughness of metallization.
- A combination of high κ and low κ materials are needed to allow for the low cost embedding of passive components into the substrate.
- The package materials will need to dissipate increasing amounts of heat generated by high power applications and higher frequency applications.

New Packaging Concepts

Packaging costs today are a substantial portion of the total device costs, hence radical new packaging concepts are needed to allow packaging costs to follow the die cost reduction curve. Some general directions that may be pursued are as follows:

- Novel new processes, structures, and interconnect are required for the next generation of devices. Evolution of flip-chip technology for instance will lead to smaller gaps and higher bump density which will necessitate improved underfills for flip chip type technologies. Eventually, a new bump-less area array technology may be needed.
- Radical solutions to provide higher wiring density through fine lines and spaces (e.g. sub 10 μm) and high bump densities are needed along with processes and production techniques that are less discrete and are more wafer-like. Such as an interconnect which can transpose from the die bump pitch directly to the board pad pitch.
- The current desired operating environment, density, operating temperature for high pad count small die, high power density and high frequency die exceed the capabilities of current assembly and packaging technology. Tighter tolerance and three dimensional control of the interconnect features are required to achieve necessary circuit performance and reliability.
- Any new packaging technology must seamlessly handle thinned die, stacked die, large and small die, and the integration of passive components either embedded or discrete. Wafer level packaging capabilities are needed.
- Biological, organic and nanostructure devices will require new packaging concepts and technologies.
- Novel package-chip systems concepts are needed to incorporate optical and electronic systems into a single cost-effective component. Models and physical design tools are needed for integration of such optical/electronic systems.

For any new packaging technology, the impact of the system on package reliability under normal use conditions and the impact of the package on the device reliability have to be investigated thoroughly for the robust device-package-system integrity and optimization. In addition to the above challenges, the major issue is the validation of thermal/mechanical models on the reliability of the device/package/system combination. This validation may be accomplished by embedded temperature and stress sensors in the device and/or package substrate. Studies related to the sensors and the feasibility of the combined structures is also needed. In general there is interest in understanding the in-situ evolution of material properties, stresses, temperature and structural integrity. Research is needed in how these may be sensed, measured and interpreted to provide meaningful inputs for predictive performance and reliability modeling and validation.

Thermal Management

Among the primary beneficiaries of advanced wafer fab technologies are microprocessors. Present microprocessor designs split the device into core logic and cache memory areas. As much as 90% of power usage occurs in the core logic area which may be only 25-50% of the total die area. The heat flux today reaches 250-300 W/cm^2 in these core logic areas. Extrapolating to future fab technology suggests that management of heat flux on the order of 500-1000 W/cm^2 will be necessary. To date thermal management of such devices has relied on the use of ever larger heat sinks and attached fans. With processors being used in products with continuingly reduced volumes (small form factor computers, thin and light notebooks, blade

servers) there is a need for new thermal management solutions with greater volume efficiency (W/cm^3) than present solutions. The same need also arises for devices with lower heat flux (<100 W/cm^2) that are used in extremely small, portable devices such as PDAs or advanced telephony devices. Thermal management solutions must account for the use of low κ insulators on the die, increased interconnect density on-chip and chip-to-package, and decreased interconnect geometries. These new materials and geometries increase the sensitivity of the packaged devices to mechanical and thermo-mechanical stress. No reduction in reliability requirements is anticipated.

Package thermal resistance (Θjc) for the high power processors is typically <0.50 °C/W. Standard measurement techniques depending on thermocouples or thermistors for measurement of reference temperatures are not sufficiently accurate for determination of thermal resistances below this level. Measurement of temperature distributions on die is also not sufficiently spatially accurate given that hotspot regions may be as small as a few microns square. New techniques for in-situ measurements on functional die are necessary for comparison to data generated using thermal test devices.

Design Analysis Tools

Coordinated design tools that integrate simulators into the design environment need to address the issue of chip, substrate and package co-design. Such a design environment must include tools for simultaneous thermal, electrical, and mechanical analysis. These tools need to provide rapid, accurate results which in turn will allow multiple design iterations. The tools must handle new 3D packaging architectures such as stacked die, stacked package, and through silicon via technologies. In the case of electrical simulation, interconnects projected to number into the tens of thousands must be analyzed. In the case of thermal analysis, smearing of Cu conductors is no longer acceptable to achieve accurate results. Both these trends lead to higher model complexities while at the same time, shorter solution times are required. Thermomechanical tools need to span scale ranges of 10000:1 easily and accurately across a wide range of material behavior models and large deformations. The availability of adequate CAD tools is one of the biggest challenges facing our industry. By and large, most on-chip CAD tools use only RC circuit representation which generates large errors in the prediction of delay variation, noise, and rise time. Designers need to learn to design controlled transmission lines in order to control the characteristics and contain the various noise sources, since noise problems will increase in severity. We need performance-driven routers and layout placement tools that rely on fast simulators in order to be able to design from the beginning, a noise free wiring configuration. After physical design, full-chip verification tools are needed for the various design iterations that include transmission line effects. For the package structures, a full-system design framework that can allow system-level signal and noise integrity analyses, DC/AC analysis of system power distribution, and EMI analyses from one common flow environment is needed. Such a framework would provide schematic entry, intuitive, graphical user interfaces, linking of modeling and simulation without file editing but with dynamic linking; easy linking to a rich library of package models that are parameterized; capability of linking to diverse set of modeling and simulation tools, from many vendors or academia, on many platforms. Such tools should operate on various parallel platforms such as Intel/P/Z servers, BlueGene, cell, multi-threaded architectures. The parallel capability is needed because for the multi-GHz era, the increase in complexity and data-rates require larger size, higher accuracy, and higher bandwidth model

generation for system performance evaluations. Full-wave effects need to be taken into account and quasi-static; analytic, approximate solutions will no longer be usable at the higher frequencies of operation. Novel hierarchical algorithmic techniques for computational electro-magnetics combined with the new parallel platforms have to be developed for the increased requirements outlined above for full-chip or full-system or sub-system analyses.

Conclusion

This "Packaging Needs" document is not intended to be inclusive, but rather to identify some of the critical areas in need of concentrated research. Other areas of needed research exist, and may be described later as needs change or updated information becomes available. Current primary thrusts continue in the realm of global interconnect, materials and interfaces, thermal management, and truly novel new packaging concepts.