Research in Support of the Die / Package Interface

Introduction

As the microelectronics industry continues to scale down CMOS in accordance with Moore's Law and the ITRS roadmap, the minimum feature size on the die decreases, BEOL (on-die) interconnect density increases, new dielectric materials are required, along with potential increases in device power and power density. The required package is also increasingly complicated in terms of number of pins, required frequency response, power delivery, power removal and thermo-mechanical stability. Many of these issues overlap between BEOL and package. Indeed, the interface between the die back-end and the package has stated to blur and as such, becomes a new area of focus. It is therefore increasingly important to optimize the total die/package sub-system, both from a functional as well as reliability performance perspective. Ideally, mechanical and electrical design of the chip and package will be done in parallel, i.e., as a co-design

However, because of the different skills and mission organization typically utilized in developing microelectronics, it is practical to examine the technical needs of the chip/package interface from two broad views: those which deal first with the physical and then second those which deal with the electrical aspects of chip/package interaction. This document therefore addresses issues relevant to the die-package interface as a mechanical subsystem in part A) and as an electrical subsystem in part B). Issues that are pertinent only to the die or only to the package have been addressed in other "needs" documents.

This document does not claim to be comprehensive in its scope. By highlighting the need for focus on the die-package interconnect, it hopes to bring about more discussion, which could lead to new research areas and new concepts.

Part A) Physical issues

The objective of this section to foster efforts that address mechanical issues of chip-to-package interconnect, heat transport, materials and mechanical reliability all as features of an integrated subsystem. As such, it should foster natural collaboration between process technologists in both die back end of line (BEOL) processing and packaging. By bridging the gap between specialized process work either on chip or package in favor of approaches that optimize the chip-package subsystem as a whole, overall mechanical integrity of the system can be optimized.

A2. Thermo-mechanical issues

A2a. Materials

A myriad of new materials are being considered to meet the requirements of smaller, higher performance packages for advanced ICs. Many of the same requirements are being faced by researchers focused on the die back end. These trends point to a need for collaboration and ideally convergence of approaches towards materials studies for both areas. The issues and the controlling material properties and mechanics are similar, while the scale in some cases may be significantly different. In addition, with the introduction of low-K materials in the die back-end, it has become evident that packaging has a significant impact on ILD reliability. Interface materials interaction including die-package material interface properties, thermo-mechanical integrity (especially of new low k materials), stress-strain characteristics, delamination, and CTE, intermetallic phase formation, electromigration, reaction kinetics, interface modification, are some examples of areas where collaborative research is needed.

A2b. Modeling

Many modeling and simulation issues are generic for chip and package, with only the geometry and the numerical values of the properties changed. The specific chip-package interface, solder balls, die attach, etc., have traditionally been handled by the package designers. But with the chip backend becoming weaker with low-k dielectrics, thermal and mechanical package deformations impose more significant displacements on the chip. The chip-package, and in some cases the chip-package-board, system needs to be considered as a whole. Comprehensive modeling from the solder mask of the package to Si BEOL structures is required, including addressing design or structural stress concentration points. Predictive tools that allow us to evaluate the robustness of the chip-package-board system and that point to locations of potential reliability failure where robustness must be increased, are essential. Radically different approaches (than the standard FEM based methods widely used in the industry) to reach the goal of solving the full die-package-board problem may be required. The need for efficient approaches to include non “linear” material properties (visco-elastic, fatigue behavior, etc) consistently and efficiently, should be pursued. Areas in need of improvement, include multi-scale modeling, transfer of geometry among fabrication, electrical, and mechanical ECAD tools, and, a standardized and practical treatment of interface reliability.

A3. Thermal management

Heat generation is a significant concern in advanced high performance ICs, and thermal management is expected to become even more critical as performance increases and system environments become more demanding. With the decreasing heat conductivity of low k dielectrics anticipated in future generations of ICs, it is increasingly important to consider their impact on interconnect self (or Joule) heating and the possible degradation of interconnect performance due to thermal issues.

Similarly the impact of the trend towards higher density current, on heat generation in the package must be considered. The standard approach of separate die and package thermal solutions is no longer appropriate. For both die and package, materials behavior under high current flux must be examined. Solutions for heat extraction are very much a complete die-package system design issue (power density, attach materials, heat spreaders, air flows, acoustics, volume constraints, etc.). Proximity effects for the entire board or system must be considered. Potential leveraging of analysis tools, methodologies and measurement metrologies must be explored. Finally, it is of great interest to explore novel cooling solutions, such as active cooling solutions, microfluidic solutions, etc.

A4. Metrology

Metrology is commonly utilized to provide accurate input data for modeling and simulation, and to assure reliable functionality in system use.

a. *Thermo-mechanical*. Measurements are needed to (1) provide the appropriate material properties, (2) detect the onset of mechanical failure (sub-um cracking and delaminations on packaged units), (3) to identify failure mechanisms and (4) to verify that the modeling has accounted for actual boundary conditions and failure modes
b. *Thermal*. Steady state and transient metrologies that enable thermal property measurements across multiple scales and validate in-situ thermal performance continue to be a challenge despite significant advances in the past few years.
c. *Failure analysis*: Fails that occur in the interface region will be increasingly difficult to isolate as the interface blurs. New techniques for probing the interface region are required.

A5. Advanced Solutions

Consideration of the chip and package as an integrated system opens up the possibilities for advanced solutions to the issues addressed by traditional interconnect and packaging designs. These include:

a. Wireless interconnect schemes to eliminate wire bonding, solder balls, conductive adhesive, or other direct electrical connections. As an example, with the clock frequencies increasing, wireless local interconnect schemes have been proposed and researched. Such an approach would require a die-package subsystem focus.
b. Three-dimensional schemes: here the partition between die and package is blurred. A subsystem approach is desired.
c. Optical interconnects for intra-chip and inter-chip communications through the package. In this scheme, an important issue is alignment of sources/receivers with the interconnects.
d. New, Out-of-the-box die-package sub-system concepts. New concepts and approaches to address systematic variations in Interconnect and Packaging, that are expected to increase due to scaling and/or increased integration

schemes. Focus is on innovative approaches to identify important process variation metrics, propose alternative interconnect processing flows and/or process modules that can be implemented in fabrication, rather than new circuit designs.

Part B) Electrical issues

The objective of this section to foster efforts that address on-chip and on-package electrical interconnect performance as integrated subsystem. As such, it should foster natural collaboration between electrical design technologists involved at the chip, package as well as system level. By bridging the functionality gap from die to system, approaches that optimize the chip-package subsystem as a whole, will provide better system

B1. Electromagnetic Modeling and Simulations.

Tools that solve Maxwell's equations have routinely been used to analyze and create RLGC models for package- and board-level interconnects. As chip performance increases, on-chip interconnects require more sophisticated RC and even RLC (or equivalent) models that require solution of Maxwell's equations in a way similar to package and board level interconnects. Even though the nature of complexity of on-chip and package interconnects may not be identical (small feature size of on-chip interconnects vs. arbitrary 3D topology of package interconnects),, with all the recent advancements in computational algorithms, appropriately designed tools for solving Maxwell's equations should be made applicable to the analysis of both the die back-end and the package interconnect space. In this way, work done for the die back-end can be leveraged for the package and vice-versa. With a single field solver for the die-package subsystem, the inherent dividing interface between die and package built into the previously separate design tools will be removed and a higher level of optimization could conceivably be obtained for the subsystem. Simulation algorithms that are inherently fast, although not necessarily as accurate as direct full-wave electromagnetic solutions, are of particular interest as a way of speeding development time and allowing multiple design iterations. A key feature that distinguishes interface tools from the independently developed on-chip or package simulation tools is that they will be of intermediate complexity and they will leverage the benefits of development from each area.

B2. Global Signals/Signal Integrity.

The same conditions as in item 1a apply here. Signal paths, both in the package and as on-die redistribution, along with the discontinuities due to vias, bumps, balls, and tortuous return paths need to be considered from the transistors outward. Handling these at the same time using the same tool might be more efficient than handling them separately and would resolve issues of potentially incompatible descriptions and tools.

Bridging these incompatibilities will help develop tools capable of assessing and optimizing system performance.

Optimized partitioning of interconnect systems in conjunction with, for example, very fine-pitch die-package connections, with multiplexed IO signals at very fast rate, with digital modulation technique in which a bit stream is serialized and then phase modulated.,

B3. Power delivery (high power/high performance chips)

As progression along Moore's Law continues, there is an overall trend to higher current and lower voltages along with potential increases in leakage power and variations. These factors produce a rapid increase in the di/dt generated noise in the chip/package sub-system, while at the same time acceptable noise margins are decreasing. This increasing impact of di/dt generated noise is seen at all levels of the power loop, from chip to package to motherboard to the voltage regulator module. This creates a critical need for improvements in technology to reduce or circumvent di/dt generated problems at all system levels.

Whereas more work on-die (such as circuit control techniques and architectural changes to limit the di/dt without sacrificing thermal demands, as well as on-chip decoupling capacitance) and on package (low inductance and low resistance, small form factor decoupling capacitor technologies) are being conducted separately, a die-package subsystem approach to deal with the power delivery issue will lead to better performance and trade-offs and lower cost.

B4. Clock distribution (high frequencies)

Increasing clock frequencies exacerbate skew and jitter problems. A die-package subsystem design approach will help alleviate them and is worthy of analysis. In addition, from a subsystem perspective, clock distribution might be better optimized through a re-evaluation of the present on-die network. Recent research in RF clock distribution is such an example.

Conclusions

With continuing advances in silicon technologies, there is an increasing coupling between the die back end and the package. This document attempts to bring this coupling into focus and discuss some examples of needed work with the goal of stimulating further discussion and, potentially, unveiling new areas of research leading to novel solutions.