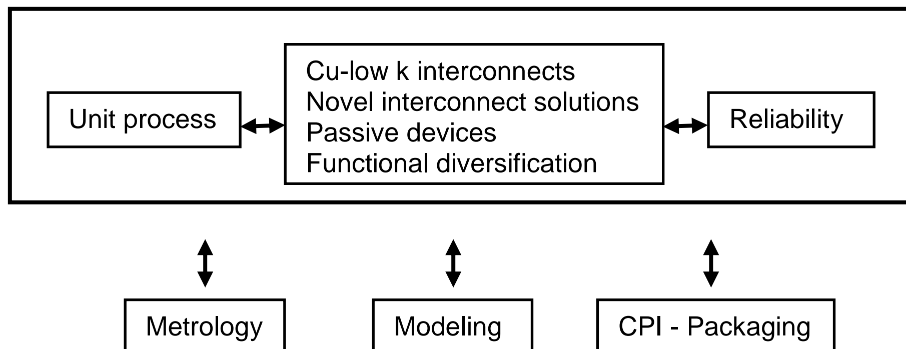
Back End Processing Needs Document

A. Introduction

This document summarizes the research needs of the SRC member companies in the area of Back End Processes (BEP), which includes experimental, simulation and metrology needs. For additional background and definitions, please refer to the 2009 ITRS Roadmap- Interconnect Chapter (http://www.itrs.net/Links/2009ITRS/IHome2009.htm).
The BEP area of interest can be grouped as follows with the interrelation shown in the figure below:

- Cu-low k extendibility
  - Metals
  - Low k dielectrics
- Unit processes
  - Metal deposition
  - Dielectrics
  - Etch and cleans
  - Planarization
- Reliability
- Advanced metrology
- Novel interconnect solutions
  - 3D integration
  - Back end of line compatible memory
  - Optical interconnect
  - Novel interconnect fabrication
  - Graphene
  - Carbon nanotubes
- Passive devices
- Functional diversification



Listed below are the core needs of SRC member companies for which experimental, simulation and metrology research are needed.

B. Cu-Low k Extendibility Research Needs

1) Metals

- Novel metallic interconnects (single element or alloys) with improved effective resistance and reliability over standard barrier/Cu interconnects.
- Alternate metal/barrier combinations with lower effective resistivity than Cu at small dimensions (< 20 nm line width).
- Physical / experimental methods to optimize and improve microstructure and interface properties and reduce the resistivity of narrow interconnects (< 20 nm line width).

2) Low k dielectrics

- Low-k, low-porosity dielectrics, including SiCOH, polymers, and other novel materials. Performance is related to the following considerations:
    - Electrical: relative permittivity (k) range of 2.0 - 2.2, low leakage, high breakdown voltage.
    - Porosity: non-porous or low porosity materials (<30%) are preferred for integration ease.
    - Low degradation during etch and cleans to maintain mechanical and electrical properties.
    - Mechanical integrity: acceptable fracture toughness, cohesive strength, residual stresses, elastic modulus, hardness, interface adhesion, and thermal expansion coefficient.
- Barriers: refer to the “Metal deposition” section (C.-1).
- Pore sealing techniques compatible with dual damascene patterning and ALD barriers, with minimal impact to the effective stack permittivity, and preserving via electrical connectivity.
- Novel techniques for recovering degradation induced by deposition, etch, and clean processes.

C. Unit Processes Research Needs

1) Metal deposition

- Bottom-up gap fill for 10:1 aspect ratios for line widths below 20 nm, with minimal overhang.
- Stand-alone barrier: thin (< 2 nm), conductive, conformal, smooth (to improve electron scattering) and “direct electro-platable” (i.e. no seed layer needed).
- Barrierless ILDs.
- Novel techniques and chemistries to fill lines and vias, including electroless plating, plating on ultra-thin seed layers, CVD, or other techniques.
- Novel techniques to improve nucleation and wetting of barrier on ILD, and Cu on barrier.
- ALD barrier approaches compatible with highly porous low-k materials

2) Dielectrics

- Novel application of dielectric materials with unique properties such as exceptionally high hardness, extremely low or high thermal conductivity, selective deposition on metal versus dielectric or vice versa, etc. for use in back end processing and applications such as patterning, heat transfer or isolation, or novel interconnect or device schemes.

3) Etch and cleans

- Fundamental understanding of plasma-surface interactions for etch, ash and cleans of low-k materials with k range of 2.0 - 2.2.
- ILD damage during etch, ash and cleans of low-k dielectrics:
    - Modifications in ILD and mechanisms responsible.
    - Techniques to repair damage created during etch and cleans; and chemical / physical processes to recover ILD k value post etch/cleans.
    - Metrology to measure sidewall dielectric damage and residues with < 1 nm resolution.
- Advanced resist / dry etch interactions:
    - Fundamental understanding and novel techniques to control and reduce LER.
    - Etch selectivity and materials integrity of photoresist and profile
- Wet chemical fundamentals: removal of resist, anti-reflecting coatings and post etch polymers without degradation of the dielectric or interfaces
- Surface preparation and cleaning techniques beyond wet and plasma cleaning, such as supercritical fluids, cryogenic aerosols, and laser cleaning.
- Plasma modeling:
    - Increased accuracy in electric and magnetic field solutions (e.g. coupled Maxwell solver)
    - Low pressure and other effects that impact species distribution and uniformity at chamber and feature length-scales.
    - Non-empirical methods to capture reactions of important species and plasma-surface interactions, to predict surface kinetics.

4) Planarization

- CMP of weak (porous or polymer) dielectrics:
    - Methods to decrease the mechanical loading during barrier removal.
    - Comprehensive understanding, including chemical, mechanical, fluid and tribological aspects to define pad, slurry and process conditions.
- Novel planarization techniques compatible with weak-dielectric/metals system with improved process control such as removal rate, defect control, etc.

D. Reliability Research Needs

- Electromigration (EM):
    - Performance of bottomless vias.
    - Methods to improve electromigration with minimum impact to electrical resistance.
- Understanding fundamentals of stress voiding and solutions to prevent it.

- TDDB understanding and methods to control leakage on plasma deposited ILDs with spaces <10 nm.
- New experimental methods to assess the mechanical integrity of stacks with multiple interconnect layers under loading conditions representative of assembly.

E. Advanced Metrology Research Needs

- Thermomechanical material metrologies for very thin films (50-150 nm), including adhesion and cohesive strength.
- Novel metrology for characterization of interfaces and sub-10nm dimensions.
- High-throughput techniques for buried void detection in copper lines and vias.

F. Novel Interconnect Solutions Research Needs

1) 3D Integration

- Novel approaches to enable high throughput deep sub-micron alignment and bonding, such as self-alignment concepts.
- Advanced materials and novel processes to enable low temperature bonding.
- Via etch, liners and fills for HAR structures.

2) Back End of Line Compatible Memory

- Novel metal and dielectric materials that could be integrated into a standard backend of line process flow for use in an embedded non-volatile memory geometries such as PCRAM, ReRAM, FeRAM, etc.

3) Optical interconnects

- On-die modulators that meet the following requirements: bandwidth higher than 30 Gb/s at 1V or lower; insertion loss below 3 dB; operation at 100 ^{o}C; compatible with Back End processing.
- Efficient couplers to send light from and into the chip.
- Light sources:
  - High power (0.3-1 W) and high efficiency lasers and laser arrays.
  - Directly modulated laser arrays capable of <30 Gb/s.
- Materials to enable Back End compatible detectors that meet the following requirements: current per unit of output capacitance above 100 mA/fF; photo/dark current ratio above 10; responsivity greater than 50 %; bandwidth higher than 30 Gb/s at 1V or lower.

4) Novel interconnect fabrication

- Alternative methods for interconnect fabrication for middle of the stack layers (~100 nm line width) to reduce processing complexity with respect to dual-damascene patterning.
- Alternatives to Cu/low k interconnects for 10-15 nm lines and vias.

5) Graphene

- Experimental benchmarking and understanding that addresses:
  - Advantages over Cu/ILD interconnects.
  - Interactions with interfaces (under and over layers, surface roughness).
  - Identification of root cause for large scattering in experimental data.

6) Carbon nanotubes

- Methods to minimize contact resistance, and selection of metal contacts.
- Controlled growth and integration of densely packed bundles.
- Understanding of scattering phenomena.

G. Passive Devices Research Needs

- High permittivity materials ($k > 20$) for decoupling capacitors.
- Magnetic materials to reduce the area of inductors.
- Materials for thin film resistors.

H. Functional Diversification Research Needs

- Explore new emerging applications such as biomedical, sensors, energy scavenging devices compatible with backend processing.