Overlapping Back End Processing and Packaging Needs Document

A. Introduction

As integration of electronics continues to increase, the demarcation between chip and package technologies is blurring. Fine line packaging is requiring the incorporation of thin film and back end of line like processes in the package structure. At the same time, three dimensional (3D) integration is pushing some technologies which previously had been considered packaging's domain into chip fabrication, such as the integration of multiple dies into a single module through wafer processing techniques. In the case of wafer scale packaging, the chip and the package are one. Additionally, electrical and thermal performance does not recognize boundaries between the chip, package or system. The strong interaction between materials selected for the package and the materials selected for the chip demand that they not be chosen in isolation. Codesign, by its very nature, is needed to optimize electrical, thermal, and mechanical performance from a chip to a package through the entire system level. In other areas, passive devices are increasingly being captured from the system board and are being incorporated into the package and chip. The architecture of the entire system needs to incorporate appropriate trade-offs between technology, cost, and performance through appropriate partitioning of functionality. The Interface area of the Interconnect and Package Sciences (IPS) group of the Global Research Corporation (GRC) aims to leverage technologies and research which addresses both chip and package concerns.

The following sections describe chip and package interface areas where the IPS would be interested in reviewing research proposals for practical technologies which can be developed and ramped to production by the 16 nm node. This document does not claim to be comprehensive in its scope. By highlighting the need for focus on the die-package interface areas, it hopes to bring about more discussion, which could lead to new research areas and new concepts.

B. Die And Package Mechanical Interactions

The drive to decrease power and delay in the interconnect stack requires introduction of new inter level dielectric (ILD) materials in every technology node. The adoption of these low-k materials typically results in decreasing strength and adhesion performance, which elevates the risk of mechanical integrity failures during assembly.

- Novel die and package solutions to decrease stress on the low-k ILDs in the interconnect stack during the assembly process.
- New experimental methods to assess the mechanical integrity of stacks with multiple interconnect layers under loading conditions representative of assembly.
- Thermomechanical material metrologies, including adhesion, cohesive strength, and detection of small cracks/delaminations (100 nm – μm range) in units (i.e. packaged die).
- Rapid and validated reliability prediction schemes (modeling).

- Alternative interconnect schemes which reduce stresses on the die.

C. 3D and Die Level Packaging

3D die and die level packaging necessitate an introduction of new materials, new process techniques, new integration schemes, and new reliability science. Electrical performance and reliability of integrated 3D die level packages and redistribution layers are not fully understood and characterized. Some key issues that would benefit from academic research include:

- Complete electrical characterization of 3D structures: Resistance, capacitance and inductance of through silicon vias (TSVs) and 3D packages versus signal frequency to 120 GHz for different via sizes and shapes. In particular cylinder, annulus, and slot designs should be considered. The performance of single vias and arrays should be addressed. The effects of the dielectric diffusion barrier, the dielectric liner, Barrier/Seed, Cu plating and anneal on RC should be explored. A fundamental LRC model for TSVs should be developed that includes voltage bias and lossy substrate effects.
- Adhesion studies focusing on the following aspects are needed: Adhesion of PVD barriers to TSV liner oxides. Adhesion of low temperature dielectrics (e.g.; nitrides, oxynitrides, carbides, or low temperature polymers) to copper. Effect of moisture on the adhesion and reliability of the metal barrier. Effect of the package and adhesives on die-to-die interactions and die-to-die adhesion.
- Reliability of 3D structures: Evaluate the dielectric liner and the metal Cu diffusion barrier performance using TDDB and BTS testing. Improved EM testing methodologies should be developed and implemented, and the TSVs characterized for EM performance under DC, AC and pulsed-currents. EM failure mechanisms should be understood. What is the effect of thermal cycling and Cu grain structures on stress migration in Cu TSVs, Cu pillars and solder joints associated with 3D die level packaging? How would the size of the vias or thickness of the solder interconnect affect reliability? What is the interaction between the TSV or redistribution layer and the dielectric stack?
- Reliability of TSVs array and the dielectric diffusion barriers: Coefficient of thermal expansion (CTE) mismatch between Cu and Si may cause protrusion and extrusion. Si cracking in dense arrays may also be a reliability concern. The failure modes and remedies should be explored. The effect of CTE mismatch on transistor performance and Si straining should be considered as well. Material alternatives, such as W should be explored.
- Thin Si deformation, buckling and warping: Develop a better understanding of the relationship of film stresses to die and/or full wafer buckling and warping in light of the anisotropic metal patterns which exist on die. The model should include multi die stacks taking into consideration the stresses at all levels, including dies, pillars, redistribution dielectrics, solder joints and adhesives. Methods to modulate stress and die and wafer deformation with thin films at various process stages should be explored.

- Low temperature and low stress bonding approaches, processes for interconnecting TSVs to redistribution layers, front and backside redistribution processing, alternative chip interconnect technologies (other than solder or metal-to-metal joining) are open to research.

D. New Passive Integration

A current trend in electronics is the incorporation of previously discrete passive components onto the die and package substrate. The IPS area of GRC is interested in Back End of Line (BEOL) technologies which enable new, denser levels of passive integration. These include:

- New BEOL capacitor structures and materials which achieve > 10x better capacitance density than currently available (> 0.5 $\mu F/mm^2$) at usable voltages (> 7 V)
- New precision resistors capable of excellent voltage, temperature and stress stability in the 0.1 - 0.5 % tolerance range. Resistance values could range from the low ohms to the mega-ohm range. TCRs should be < 25 ppm/° C.
- BEOL technologies which could lead to high "Q" integrated inductors (Q > 50) in the > 100 nH/mm^2 range.

E. Functional Diversification

3D interconnection technologies allow the integration of multiple process technology devices into an individual package. Logic, memory, analog, RF, optics, MEMS, and bio devices will be combined together for form monolithic systems or subsystems. Novel interconnect schemes are sought to link these devices. Medical electronics require new ways to interface electronics with biological systems. Wafer level packaging of MEMS component technologies is sought.

- Lower temperature interconnect technologies to link devices such as labs on a chip, which can't withstand high temperature steps, to other electronics in the module.
- Wafer level MEMS packaging technologies for accelerometers, RF switches, microphones, etc.
- Technologies to link electronic components to biological systems for neural stimulation such as pain management systems, retinal prosthesis, or cochlear implants.

F. Thermal Management

The challenges of thermal management have been shifted from macroscopic level to microscopic level due to geometry shrinks and the continuous reduction of the Si die size. In addition, the radical change of end-user customer applications creates higher utilization rates for active die blocks. There is a great challenge to thermally manage the next generation of packaging where the power will be switched on/off at high frequency to reduce the power consumption.

There is a great interest to understand:

- New approaches of thermal management in the transient phase between different metal layers and interconnects with a better understanding of the future end-user applications and the energy saving
- Development of thermal management techniques which account for the impact of thermo-mechanical stress and electromigration
- Novel low cost super thermal spreading techniques on the package or die to be in contact with the system level thermal management structures
- Development of high thermally conductive passivation, underfill and non-conductive adhesives (> 10 W/m-° C) to enhance thermal management inside the Si and the package.
- Novel thermal management techniques to address the challenges in the stacked-die
- Thermal imaging or metrology of localized circuit hot spots at the near nano-scale level
- Phonon and electron transport based thermal modeling for small length scales where continuum assumptions may not be applicable

G. Conclusions

With continuing advances in silicon technologies, there is an increasing coupling between the die back end and the package. This document attempts to bring this coupling into focus and discuss some examples of needed research with the goal of stimulating further discussion and, potentially, unveiling new areas leading to novel solutions.