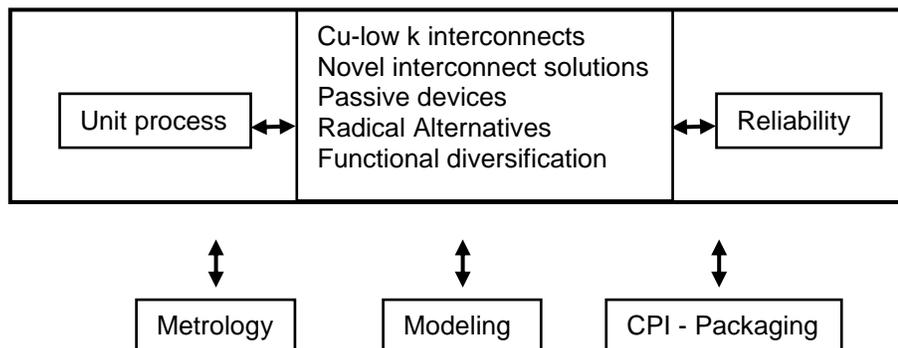


Back End Processing Needs Document

Introduction

This document summarizes the research needs of the SRC member companies in Back End Processes (BEP) and related science areas. For additional background and definitions, please refer to the 2009 ITRS Roadmap-Interconnect Chapter (<http://www.itrs.net/Links/2009ITRS/IHome2009.htm>).

The general BEP areas of interest:



Detailed core needs of SRC member companies for which experimental, simulation and metrology research are needed:

A. Cu-Low k Extendibility Research Needs

1) Metals

- Novel metallic interconnects (single element or alloys) with improved reliability over standard barrier/Cu interconnects.
- Alternate metal/barrier combinations to lower interconnect resistances at small dimensions (< 20 nm line width).
- Physical / experimental methods to optimize and improve microstructure, interface properties and integrity of Cu lines in sub-20nm features.

2) Low k dielectrics.

- Ultra Low-k (ULK) dielectrics, including porous SiCOH and other novel materials. Performance is related to the following considerations:
 - Electrical: relative permittivity (k) range of 2.4 or less, low leakage, high breakdown voltage.
 - Low degradation during etch and cleans to maintain mechanical and electrical properties.

- Mechanical integrity: acceptable fracture toughness, cohesive strength, residual stresses, elastic modulus, hardness, interface adhesion, and thermal expansion coefficient.
- Pore sealing techniques compatible with dual damascene patterning and CVD/ALD barriers, with minimal impact to the effective stack permittivity, and preserving via electrical connectivity.
- Novel techniques for recovering degradation (surface and bulk) induced by deposition, etch, and clean processes.

B. Unit Processes Research Needs

1) Metal deposition

- Stand-alone barrier or liner: novel precursors and chemistries to deliver a thin (< 2 nm), conductive, conformal, smooth (to improve electron scattering) and plate-able film.
- Novel techniques and chemistries to fill high aspect ratio, sub-20nm lines and vias, including electroless plating, CVD, PVD or other techniques.
- Novel techniques to improve nucleation and wetting of barrier on ILD, and Cu on barrier.
- ALD barrier/seed approaches compatible with highly porous low-k materials.
- Selective deposition on copper vs. dielectric.

2) Dielectrics

- Novel application of dielectric materials with unique properties such as exceptionally high hardness and elastic modulus, extremely low or high thermal conductivity, selective deposition on metal versus dielectric or vice versa, etc. for use in back end processing and applications such as patterning, heat transfer or isolation, or novel interconnect or device schemes.
- Liner-less, Cu diffusion resistant ILDs to improve line and via resistance, and extend gap fill to smaller dimensions.

3) Etch and cleans

- Fundamental understanding of plasma-surface interactions for etch, ash and cleans of low-k materials with k in the range of 2.4 or less.
- ILD damage during etch, ash and cleans of low-k dielectrics:
 - Characterization and fundamental modeling of the changes (physical and chemical) in the ILD caused by different processing steps.
 - Techniques to repair damage created during etch and cleans; and chemical / physical processes to recover ILD k value post etch/cleans.
 - Metrology to measure depth and composition of sidewall dielectric damage and residues with < 1 nm resolution.
- Advanced resist / dry etch interactions:
 - Fundamental understanding and novel techniques to control and reduce LER.
 - Etch selectivity and materials integrity of photoresist and profile
- Wet chemical fundamentals: removal of resist, anti-reflecting coatings and post etch polymers without degradation of the dielectric or interfaces

- Surface preparation and cleaning techniques beyond wet and plasma cleaning, such as supercritical fluids, cryogenic aerosols, and laser cleaning.
- Plasma modeling:
 - Low pressure and other effects that impact species distribution and uniformity at chamber and feature-length scales.
 - Non-empirical methods to model plasma species reactivity (gas phase and surface) to help guide plasma chemistry development.

4) Planarization

- CMP of porous dielectrics:
 - Methods to decrease the mechanical loading during barrier removal.
 - Comprehensive understanding, including chemical, mechanical, fluid and tribological aspects to define pad, slurry and process conditions.
- Novel planarization techniques compatible with weak-dielectric/metal (including noble metal liners such as Ru, Co) systems with improved process control such as removal rate, defect control, etc.

C. Reliability Research Needs

- Electromigration (EM):
 - Methods to improve EM with minimum impact to electrical resistance.
 - Cu alloying, liner interactions, adhesion and interface diffusion.
 - Improved Cu microstructure, plating defects
 - Short length effects in dual damascene sub-20nm lines.
 - Alternative techniques to enable rapid EM characterization
- Understanding fundamentals of stress voiding
 - Role of microstructure, temperature cycling, interface control
 - Stress relaxation mechanisms and relation to void nucleation and growth
- TDDB mechanisms and methods to control leakage on plasma deposited ILDs with spaces <30 nm.
 - Role of capping layer, CMP residuals, copper migration
 - Field dependence, acceleration factors, soft/hard breakdown mechanisms
- New experimental methods to assess the mechanical integrity of stacks with multiple interconnect layers under loading conditions representative of assembly.
- Variability modeling - quantify relative impact of variations in processing, feature geometry on reliability.

D. Advanced Metrology Research Needs

- Thermomechanical material metrologies for very thin films (50-150 nm), including adhesion and cohesive strength.
- Novel metrology techniques for characterization of surfaces, interfaces and sub-10nm dimensions.
- High-throughput techniques for buried void detection in copper lines and vias.
- High resolution analysis of electromigration and stress migration damage sites.

- Time resolved grain structure evolution during copper recrystallization in narrow lines.
- New analytical techniques with high spacial resolution and chemical sensitivity: Doping, impurity levels at interfaces and within narrow features

E. Novel Interconnect Solutions Research Needs

1) 3D Integration

- Novel approaches, advanced materials and processes to enable high throughput, low temperature deep sub-micron alignment and bonding, such as self-alignment concepts.
- Via etch, liners and fills for HAR (high aspect ratio) structures.
- Reliability in 3D package environment
 - Effects of TSV processing on BEOL reliability

2) Back End of Line Compatible Memory

- Novel metal and dielectric materials that could be integrated into a standard backend of line process flow for use in an embedded non-volatile memory geometries such as PCRAM, ReRAM, FeRAM, etc.
- Interconnect centric memory; e.g., cross point memory, HAR contacts and vias, BEOL memory integration.

3) Optical interconnects

- On-die modulators with high bandwidth (30 Gb/s at 1V or lower), low insertion loss (below 3 dB), operation at 100 °C, and compatible with Back End processing.
- Efficient couplers between chip, package and/or interposers
- Materials to enable Back End compatible detectors that meet the following requirements: current per unit of output capacitance above 100 mA/fF; photo/dark current ratio above 10; responsivity greater than 50%; bandwidth higher than 30 Gb/s at 1V or lower.

4) Novel interconnect fabrication

- Alternatives to Cu/low k interconnect processing for 10-15 nm lines and vias.
- Emerging technologies – modeling and simulation, property verification

F. Passive Devices Research Needs

- High permittivity materials ($k > 20$) for decoupling capacitors.
- Magnetic materials to reduce the area of inductors.

G. Functional Diversification Research Needs

- Explore new emerging applications, such as biomedical, sensors, energy scavenging devices compatible with backend processing.