

IPS - Interface: Processing Needs Document

Introduction

The Interconnect Packaging Sciences has identified the interface between Back End Processing and Packaging as a critical area to the extension of semiconductor processing to the 16nm technology node and beyond. Below is a table highlighting the key areas of interest for back end processing and packaging, as well as key areas at the interface of the two thrusts.

<u>Back End Processing</u>	<u>Interface between BEP and PKG</u>	<u>Packaging</u>
Cu-Low k Extendibility ▪ Unit Level (Module) Processing ▪ Reliability ▪ Advanced metrology ▪ Alternate/Novel Concepts	Die/Package Mech. Interactions ▪ Die Level Packaging & 3D ▪ Passive Devices ▪ Thermal Management ▪ Functional Diversification	Materials and Interfaces ▪ Thermal Solutions ▪ Reliability ▪ High Frequency I/O ▪ Novel Concepts

Below is a more detailed description of the interest areas for the interface region. It serves to highlight the needs of SRC member companies and where experimental, theoretical, or analytical research is needed from the academic community.

A. Die And Package Mechanical Interactions

- Novel die and package materials and schemes that decrease stress on the low-k ILDs in the interconnect stack during the assembly process.
- Development of novel metrologies or analytical techniques to:
 - Assess the mechanical stress applied by the package interface on multilevel interconnect structures.
 - Assess the strength of the interconnect stack under loading resembling those applied by the package at assembly.
- Model or experiment based approaches that predict the reliability of the die-package interface.
- Alternative interconnect materials and schemes which reduce stresses on the die.

B. 3D and Die Level Packaging

- Systematic adhesion studies and adhesion metrology development for different interfaces in the TSV scheme:

- PVD barriers to TSV liner oxides, low temperature dielectrics to copper, etc.
- The effect of environment (i.e. moisture/temperature) on the adhesion and reliability of the metal barrier.
- Studies on the effects of the packaging and adhesives on die-to-die interactions and die-to-die adhesion.
- Detailed study of the reliability of 3D structures as a function of process variations:
 - a. Fundamentals of TDDDB in TSVs .
 - b. Alternative techniques to enable rapid EM characterization and identify key EM failure mechanisms
 - c. Investigation into the effects of thermal cycling and Cu grain structures on stress migration in Cu TSVs and solder joints.
 - d. Interactions between the TSV or redistribution layer and the dielectric stack.
 - e. Role of coefficient of thermal expansion (CTE) mismatch between fill material (Cu or other novel materials) and Si that causes protrusion and extrusion, including effects on transistor performance.
- In depth studies of thin Si deformation, buckling and warping in order to understand the relationship of film stresses to die and/or full wafer.
- Development of novel metrologies to identify bonding voids in 3-D stacking schemes.
- Low temperature and low stress bonding materials for interconnecting TSVs to redistribution layers.

C. New Passive Integration

- New back-end capacitor and electrode materials that achieve > 10x better capacitance density than currently available (> 0.5 $\mu\text{F}/\text{mm}^2$) at usable voltages for logic devices.
- New precision resistors capable of excellent voltage, temperature and stress stability in the 0.1 - 0.5 % tolerance range.
- New materials that lead to high “Q” integrated inductors ($Q > 50$) in the > 100 nH/mm² range.

D. Thermal Management

- Novel techniques for thermal management at the interface between interconnects and packaging.
- Novel low cost thermal spreading techniques on die to be in contact with the system level thermal management structures
- Novel thermal management techniques for back-end-of-line
- Development of novel thermally conductive passivation, underfill and non-conductive adhesives (> 10W/m-°C) to improve thermal management inside the Si and the package.
- Thermal imaging or metrology of localized circuit hot spots at the near nano-scale level

- Phonon and electron transport based thermal modeling for small length scales where continuum assumptions may not be applicable

E. Functional Diversification

- Explore novel on-die, non-logic applications such as sensors, MEMs, biomedical, RF switching, and energy applications.
- Enabling technologies such as low temperature interconnect schemes.
- Wafer level packaging for MEMS technologies such as accelerometers, RF switches, microphones, etc.