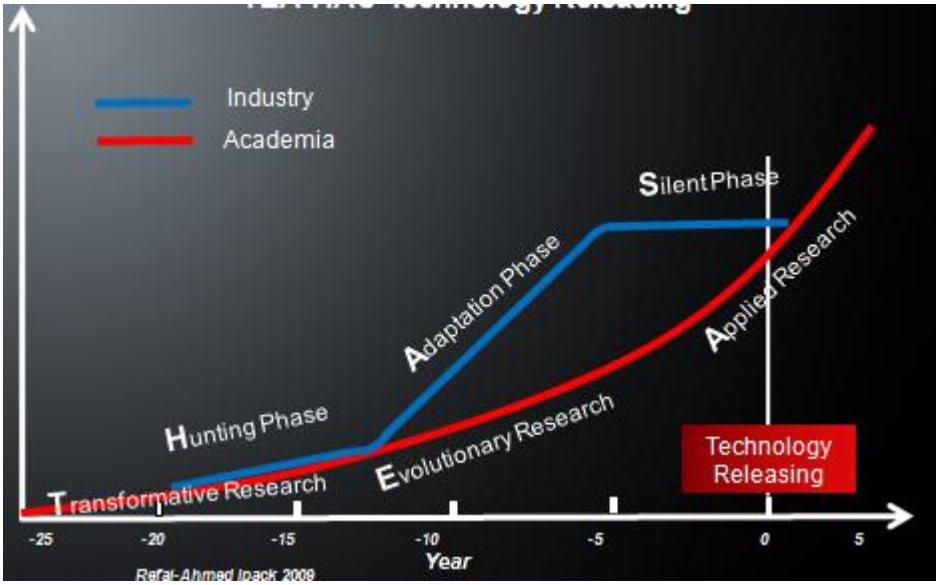
Packaging Needs Document

A. Introduction

Processing architectures need to continue to take advantage of silicon technology dimensional scaling to provide performance enhancements, but with increasingly severe system power limits. This will make it increasingly difficult to obtain performance growth without innovation in packaging technology. We have entered an era of the convergence of three major challenges that will shape the direction in packaging for the next decade: escalating power densities in constrained system environments, the need to provide increasing bandwidth, and chip-package interaction issues. Increased component and system power density in constrained environments appears unavoidable, with attendant thermal management issues, including both global difficulties and hot spots. Expanded use of multi-core architecture to mitigate processor power drives exponential growth in demand for bandwidth which cannot be satisfied by simply scaling conventional two dimensional packaging, fueling demand for new integration schemes like 3D integration. Silicon materials innovations to offset power include ever lower dielectric constant insulators, typically offering interconnect with reduced fracture toughness. This in turn places enormous emphasis on understanding the thermal, mechanical and electrical interaction of the chip and package as well as the package and system.

The GRC division of SRC focuses on research in a timeframe 5-14 years ahead of technology release. As described in the graphic below (Refal-Ahmed, Ipack 2009), this typically corresponds to the evolutionary research phase for academia and adaptation phase for industry. This phase represents the “sweet spot” for pre-competitive collaborative research, after which the industry focuses on proprietary development for technology differentiation by their respective companies. Successful research proposals will need to match this timing.



In this document we attempt to highlight some of the key strategic challenges facing packaging technology. Against each of these challenges, the industry requires basic

and fundamental understanding of the underlying science in a form that can be easily applied to real engineering solutions. Research project proposals specifically addressing the following science areas are welcome for consideration.

B. Global Interconnects

Packaging plays a critical role in enhancing system performance where inter-component connectivity is just as important as individual component performance. The packaging challenge is to develop high bandwidth interconnections between components. High bandwidth is provided both by enabling low loss interconnect and by increasing the number of connections between system components in a cost effective manner. There is a strong need to develop new packaging architectures and also to enable and evaluate high speed performance of the global interconnects between system components for existing packaging architectures. The scope of this effort includes modeling and validation to improve the overall predictability of interconnects performance. Specific areas of interest are for proposals that

- Identify new packaging and system architectures, including optical interconnects, for improved on package, per socket and overall system bandwidth
- Identify modeling methodologies that will help to significantly improve modeling accuracy and/or significantly reduce computation speed without loss of accuracy and without compromises on important physical effects
- Develop validation methodologies and experimental techniques for material, component and system characterization.

C. 3D Stacked Die

There is growing interest to find alternatives to scaling that allow the performance to continue increasing from one generation to another. Therefore, 3D stacked die was established as a focus area in both the SRC and the ITRS roadmaps to accomplish this goal. It is very important to establish clear research areas on 3D. These topics need to be investigated by researchers with specific goals and deliverables so that the results can be transfer to the industrial side in its technology/product roadmap. The following areas are of particular interest:

- Design envelope definition of 3D silicon stacks with Through Silicon Vias (TSV).
- Establish the physics based failure modes of TSVs in 3D silicon stacks due to accumulated damage.
- Establish the flow of Non Conductive Adhesives (NCA) and underfills used in 3D silicon stacks with TSV.
- Establish critical variables affecting the fracture toughness of thinned silicon used in 3D stacks with TSV.
- Fabricate and perform electrical, thermal, and mechanical modeling and measurements of 3D interconnects including:
    - Novel fabrication of TSVs with various dimensions, aspect ratios, cross-sectional shapes, and dielectric layer thickness.
    - Resistance, capacitance, and inductance measurements and modeling
    - Mechanical/thermo-mechanical modeling and testing, including micro-Raman measurements and beam bending

- Investigate the main factors that impact the electromigration on the Chip-Packaging Interaction such as:
    - Interaction of TSV structures
    - Multilevel modeling of CPI for low k chip with TSVs
    - Electromigration and stress reliability of TSV contacts as a function of geometry and temperature
    - Design, fabrication, test methodology of test structures to measure electromigration
- Understand the different Power Delivery architectures on the stacked ICs and Packages with TSVs through:
    - Exploring the interaction of the power delivery on different stacked-die packaging architecture
    - Developing and verifying different modeling approaches of the power delivery in IC
    - Co-design of the power delivery network in 3D ICs and the trade-offs between chip area needed for power/signal/TSVs
- Novel 3D architecture based on stacking of multiple processors and memory IC with innovative interconnect including:
    - new thermal management techniques to address hotspots, Joule heating and thermo-mechanical stresses
    - solid state cooling, micro-channel based and other cooling solutions

D. Thermal Management

Continued exploitation of multi-core processors coupled with scaling will drive local power density and the attendant need to manage local “hot spots”. Modeling, measuring, and mitigating the effects of hot spots continues to be of interest. Novel cooling techniques such as advanced solid state refrigeration as well as conjugate heat transfer for high performance need to be understood. Mechanisms for degradation in thermal performance, notably at thermal interfaces, need to be explored, with development of predictive methodologies. High speed thermal models, accurate transient and steady state metrologies and efficient thermal solutions need to be addressed for both 2D and 3D applications. These applications include structures where several “hot” die are stacked, as well system level considerations, such as board-level heat dissipation. Coupled with the continuous drive towards miniaturization due to the explosion of mobile devices, reliable and affordable thermal management technology remains a major packaging challenge. Of particular interest are:

- Hot spot metrology and mitigation schemes
- Predictive reliability methodologies for thermal interfaces
- Modeling and thermal management strategies for 3D applications
- Novel cost effective solutions for high power density mobile applications

E. Materials and Interfaces

Advances in materials, materials science, formulation methods, and process methods continue to be integral to the development of new package concepts. New materials, materials knowledge and processes are needed with an eye to practical implementation to enable industry growth. Novel materials and processes for passive integrated

devices either on the die, in the substrate, or in the package will enable next generation heterogeneous system integration. Higher dielectric constant materials and practical processes to enable stable super capacitors or thin film batteries in a package are desired, as are high permeability integration schemes for in-package high density inductors. Coatings or other materials and techniques to enable biocompatibility are desired for the development of directly implantable systems. Metrology which quickly and quantitatively characterizes interfacial behaviors such as adhesion and sub-critical de-bonding under a wide range of environmental temperature and humidity conditions continues to be needed for a priori evaluation of material suitability for packaging applications and improved predictive reliability. Fundamental understanding of packaging materials and interface systems such as interface fatigue behavior and thermal resistance is needed to enable the industry to design materials tailored for package needs. Of particular interest are:

- Novel materials and processes for redistribution layers or passive integration on chip, in substrate, or in package
- New fast metrology methods for interfacial adhesion, fatigue, de-bonding under wide humidity and temperature ranges, and for stress and displacement evolution as a function of process and operating conditions.
- Fundamental understanding of package material interactions such as interfacial behavior and thermal resistance
- Near hermetic or biocompatible coatings

F. New Concepts

Revolutionary concepts are sought to enable the electronics industry to reach new levels of integration in the coming decade. New applications for electronics are developing, from implantable retina prosthesis, to direct brain stimulation, to cochlear implants, to pain management, to wearable electronics, to wireless everywhere, to energy scavenging, to millimeter wave and terahertz packaging. Radical low cost packaging solutions enabling very high density systems are demanded. Innovative chip integration and interconnect techniques for on chip stacking, in the substrate embedding, chip in PCB, and chip on flex are needed. Materials which can be demonstrated to enable novel interconnection technologies should be developed with supporting metrology for thorough characterization. New methods of package design, architecture, and system partitioning for traditional and non-traditional system applications are welcome. Of particular interest are:

- Revolutionary package concepts for heterogeneous integration
- Novel interconnection schemes
- New package design architectures and system partitioning with analysis tools

G. Conclusion

This “Packaging Needs” document is not intended to be inclusive, but rather is intended to identify the critical areas in need of concentrated research. Other areas of needed research exist, and may be described later as needs change or updated information becomes available. Current primary thrusts continue in the realm of global interconnect, materials and interfaces, thermal management, novel packaging concepts, with a major new thrust in 3D integration.