Packaging Needs Document

Introduction

Processing architectures need to continue to take advantage of silicon technology scaling to provide performance enhancements but with increasingly restrictive system power limits. This will make it increasingly difficult to obtain performance enhancement without innovation in Packaging technology. The industry have entered an era of the convergence of three major challenges that will shape the direction of Packaging for the next decade: escalating power densities in constrained system environments, the need to provide increasing bandwidth, and chip-package interaction issues. Increased component and system power density in constrained environments appears unavoidable with attendant power delivery (requiring fast responding power delivery networks) and thermal management (requiring power and form factor efficient global and hot spot cooling) issues. Expanded use of multi-core architecture to mitigate processor power drives exponential growth in demand for bandwidth which cannot be satisfied by simply scaling conventional two dimensional packaging fueling demands for new integration schemes like 2.5D and 3D integration. Silicon material innovations to offset power include ever lower dielectric constant insulators, typically offering interconnect with reduced modulus, hardness and fracture toughness. This in turn places enormous emphasis on understanding the thermal, mechanical and electrical interaction of the chip and package as well as the package and system.

The GRC division of SRC concentrates on research activities in a timeframe of 5-14 years ahead of technology release. Interconnect and Packaging Sciences division of GRC focuses on creating and exploring advanced evolutionary, revolutionary, and transformative technologies for connecting elemental devices (transistors, capacitors, nano-devices, etc.) to each other and to the macro world targeting the 8 nm technology node and beyond, including 3D and heterogeneous integration and facilitating strong bridges and foster new ideas between the Packaging and Interconnect communities .Areas of continued emphasis include new 3D architectures, Optical I/O research and Novel interconnect/dielectric materials & processing research.

This document primarily highlights some of the key strategic challenges facing Packaging technology. For each of these challenges, the industry requires basic and fundamental understanding of the underlying science in a form that can be easily applied to real engineering solutions. Research project proposals specifically addressing the following science areas are welcome for consideration.

1. Global Interconnects

Packaging plays a critical role in enhancing system performance where inter-component connectivity is just as important as individual component performance. The packaging challenge is to develop power efficient high bandwidth interconnections between components. High bandwidth is provided both by enabling low loss interconnect and by increasing the number of connections between system components in a cost effective manner. There is a strong need to develop new packaging architectures and also to enable

and evaluate high speed performance of the global interconnects between system components for existing packaging architectures. The scope of this effort includes modeling and validation to improve the overall predictability of interconnect performance. Specific areas of interest for proposals include the following which identify and develop,

- New packaging and system architectures, including optical interconnects for improved package per socket, overall system bandwidth and input/output power efficiency.
- Modeling methodologies that will help to significantly improve modeling accuracy and/or significantly reduce computation speed without loss of accuracy and without compromises on important physical effects.
- Validation methodologies and experimental techniques for material, component and system characterization.

2. Power Delivery

Future power delivery applications are expected to require 5-10A/mm^2 at 1V or less; and there is a need to develop solutions to meet this demand. There is also a drive to smaller form factors so the power delivery solutions should fit within the same footprint, be they on the package and/or die, and have a small z-height. Moving forward, electronic systems need to have low resistance chip-to-chip and chip-to-package interconnects capable of delivering high power/current densities with no/minimal electromigration.

Specific areas of interest for research proposals include,

- High density, low impedance capacitors and high efficiency inductors.
- Voltage regulator technologies such as inductor based or switched capacitor. The voltage regulators should be able to regulate the output voltage to the range of 0.3V to 1.0V. The overall efficiency of the regulator, including transistor and passive losses, should be in the 90+% range. Conversion ratios for input to output voltage can cover a wide range from small values of 1.2:1 to 8:1
- Proposals on novel power delivery solutions are also welcome.
- New materials and Interconnect systems capable of delivering high power with no /minimal electromigration.

3. 3-D Stacked Die

There is growing interest to find alternatives to scaling that allow the performance to continue to improve from one generation to another. 3-D stacked die was established as a focus area in both the SRC and the ITRS to sustain generational performance improvements. It is very important to establish clear research areas on 3-D. These research topics need to be pursued with specific goals and deliverables so that the results can be transferred to the

industry and be included in their technology/product roadmaps. The following areas are of particular interest:

- Design envelope definition of 3D silicon stacks with Through Silicon Vias (TSVs).
- Establish the physics based failure modes of TSVs in 3D silicon stacks due to accumulated damage.
- Establish the flow of Non Conductive Adhesives (NCAs) and underfills used in 3D silicon stacks with TSVs.
- Establish critical variables affecting the fracture toughness of thinned silicon used in 3D stacks with TSVs.
- Fabricate and perform electrical, thermal, and mechanical modeling and measurements of 3D interconnects including:
    - Novel fabrication of TSVs with various dimensions, aspect ratios, cross-sectional shapes, and dielectric layer thickness.
    - Ballistic Electrical and Thermal transport capable fill materials including CNT's and nanowires.
    - Resistance, capacitance, and inductance measurements and modeling.
    - Mechanical/thermo-mechanical modeling and testing, including micro-Raman measurements and beam bending.

- Investigate the main factors that impact the electromigration on the Chip-Packaging Interaction (CPI) such as:
    - Interaction of TSV structures.
    - Multilevel modeling of CPI for low dielectric constant (k) chips with TSVs.
    - Electromigration and stress reliability of TSV contacts as a function of geometry and temperature.
    - Design, fabrication and test methodology of test structures to measure electromigration
- Understand the different Power Delivery architectures on stacked ICs and Packages with TSVs through:
    - Exploring the interaction of the power delivery on different stacked-die packaging architectures.
    - Developing and verifying different modeling approaches of the power delivery in ICs.
    - Co-design of the power delivery network in 3D ICs and the trade-offs between chip areas needed for power/signal/TSVs.
- Novel 3D architecture based on stacking of multiple processors and memory ICs with innovative interconnect including:
    - New thermal management techniques to address hotspots, Joule heating and thermo-mechanical stresses.
    - Solid state cooling, micro-channel based and other cooling solutions.
    - New thermally optimized 3D architectures for asymmetrically partitioned assembled 3D Systems.

4. Thermal Management

Continued exploitation of multi-core processors coupled with scaling will drive local power density and the attendant need to manage local "hot spots". Modeling, measuring, and mitigating the effects of hot spots continues to be of interest. Novel cooling techniques such as advanced solid state refrigeration as well as conjugate heat transfer for high performance need to be understood. Mechanisms for degradation in thermal performance, notably at thermal interfaces, need to be explored, with development of predictive methodologies. High speed thermal models, accurate transient and steady state metrologies and efficient thermal solutions need to be addressed for both 2D and 3D applications. These applications include structures where several "hot" die are stacked, as well system level considerations, such as board-level heat dissipation. Coupled with the continuous drive towards miniaturization due to the explosion of mobile devices, reliable and affordable thermal management technology remains a major packaging challenge. Of particular interest are:

- Hot spot metrology and mitigation schemes.
- Predictive reliability methodologies for thermal interfaces.
- Modeling and thermal management strategies for 3D applications.
- Novel cost effective passive solutions for mobile applications.
- Form factor restricted thermal solutions to meet both reliability and ergonomic requirements.

5. Materials and Interfaces

Advances in materials, materials science, formulation methods, and process methods continue to be integral to the development of new package concepts. New materials, materials knowledge and processes are needed with an eye to practical implementation to enable industry growth. Novel materials and processes for passive integrated devices either on the die, in the substrate, or in the package will enable next generation heterogeneous system integration. Higher dielectric constant materials and practical processes to enable stable super capacitors or thin film batteries in a package are desired, as are high permeability integration schemes for in-package high density inductors. Coatings or other materials and techniques to enable biocompatibility are desired for the development of directly implantable systems. Metrology which quickly and quantitatively characterizes interfacial behaviors such as adhesion and sub-critical de-bonding under a wide range of environmental temperature and humidity conditions continues to be needed for evaluation of material suitability for packaging applications and improved predictive reliability. There are reliability challenges associated with packaging of extremely large and thin dies especially for 3 D Packaging systems and packaging materials need to be developed or modified to have reliable compliant Packages. Fundamental understanding of packaging materials and interface systems such as interface fatigue behavior and thermal resistance is needed to enable the industry to design materials tailored for Package needs. Of particular interest are:

- Novel materials and processes for redistribution layers or passive integration on chip, in substrate, or in package.

- New fast metrology methods for interfacial adhesion, fatigue, de-bonding under wide humidity and temperature ranges and for stress and displacement evolution as a function of process and operating conditions.
- Fundamental understanding of package material interactions such as interfacial behavior and thermal resistance.
- Near hermetic or biocompatible coatings.
- Novel package substrate materials that enable ultrafine pitch (Sub 40um) bump architectures, Ultra thin packages, transparent electronics etc.
- Development of complaint package designs and materials for very large ultrathin dies including stacked dies.
- Bump replacement materials (Nanowoires etc.) for sub 10um pitch bumps.

6. New Concepts

Revolutionary concepts are sought to enable the electronics industry to reach new levels of integration in the coming decade. New applications for electronics are developing, from implantable retina prosthesis to direct brain stimulation, cochlear implants, pain management, wearable electronics, wireless everywhere, energy scavenging, and millimeter wave and terahertz packaging. Radical low cost packaging solutions enabling very high density systems are demanded. Innovative chip integration and interconnect techniques for on chip stacking, in the substrate embedding, chip in PCB, and chip on flex are needed.

Materials which can be demonstrated to enable novel interconnection technologies should be developed with supporting metrology for thorough characterization. New methods of package design, architecture, and system partitioning for traditional and non-traditional system applications are welcome. Of particular interest are:

- Revolutionary package concepts for heterogeneous integration.
- Novel interconnection schemes.
- New package design architectures and system partitioning with analysis tools.
- Package Design for flexible and wearable electronics.
- Small form factor flexible packaging designs.
- Package Design for bio- compatible electronics.

Conclusion

This “Packaging Needs” document is not intended to be inclusive, but rather to identify the critical areas in need of concentrated research. Other areas of needed research exist and may be described later as needs change or updated information becomes available. Current primary thrusts continue in the realm of global interconnect, materials and interfaces, thermal management, novel packaging concepts, with a major new thrust in 3D integration.