Research Needs Document: Logic and Memory Devices

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Background

This document is prepared to accompany the Call-for-White-Papers for the thrust of Logic and Memory Devices. The research needs in this area are very wide. We present here selected areas of high priorities as identified by our sponsor members.

In an integrated circuit, transistors and memories are the most important and common components. For transistors, the natural progression beyond the current manufacturing technologies, SOI planar MOSFETs and FinFETs, will be nanowire MOSFETs, all based on Si channel materials. Other than these Si MOSFET structures, there are potential benefits to be gained by going to other alternate channel materials with high mobilities, such as different versions of III-V compounds, Si_xGe_{1-x} compound or pure Ge, graphene, carbon nanotube, 2-D crystals, etc. It is believed that even though mobility is a low-field phenomenon, its more favorable scattering process can lead to higher high-field saturation velocity or ballistic velocity, which in term can result in larger current.

Common MOSFET devices encounter one common fundamental limitation of MOSFET principle–a subthreshold slope of 60 mV/decade. This places a lower limit on the operational voltage given the required on-current to off-current ratio. There is a group of logic devices that based on different material and device physics and can lead to subthreshold slope steeper than this fundamental limit. A few approaches are being examined. One is based on gate-control tunneling as in tunnel FET (TFET), because tunneling is not limited by the *kT/q* factor. Another is to use ferroelectrics as gate oxide in MOSFET. The abrupt polarization in ferroelectrics induces internal voltage partition between that in oxide and in the channel. This phenomenon is sometime referred to as negative capacitance. It is important to notice that both of these examples have a structure that is similar to a MOSFET, even though their operation principles are quite different. This feature adds value in that the fabrication is compatible with Si MOS process, and within the process capability of university research. Other examples in this group include piezoFET (based on piezoelectric effect) and IMOS (based on impact ionization).

Lastly, logic devices have been pursued based on totally different materials and physical phenomena. This class of novel logic devices have been called beyond CMOS. Examples are spin-based devices, nanomagnets, phase transition devices (metal-insulation transition), etc. This class of devices are disruptive technology and impactful to the semiconductor industry. They are high-risk and call for more innovative research that is especially suitable for university research.

For memories, they are classified into major categories of nonvolatile memories (NVMs), SRAM, and DRAM. Each has its trade-offs in different aspects of performance, has its unique feature and structure, but all are critical to the industry. For NVMs, the industry has been depending on the charge-storage type, which are floating-gate FET and charge-trapping FET. However, both of these devices have a tunnel gate oxide at the channel interface, but due to the stringent requirement of long retention time, this tunnel oxide is already at its minimum thickness and is no longer scalable. The industry has started to turn to non-charge-storage type of memory cells that are typically two-terminal. Examples are STTRAM, ReRAM, PCRAM, etc. However, the on-state characteristics of these cells typically exhibit *I-V* characteristics that are too conducting at low bias, and provide leakage paths in a memory array. To control this short-coming, a selection device is needed in series. This makes the memory cell a two-element cell, so it is desirable to have a selection device that is two-terminal rather than three-terminal (transistor) that requires a larger area. However, a good selection device that meet all the requirements has not been demonstrated.

Research Needs

The research needs for logic and memory devices are obviously very wide. In this call, due to limited resources, we have gone through some discussions and have identified what our members have considered the most critical and relevant for university research. The list of topics are shown below, and more-detailed explanation for each follows:

1) Logic devices:
   1a) Beyond CMOS devices. Use of novel materials, phases, and phenomena to demonstrate new class of computing devices.
   1b) MOSFET-like structures with steep subthreshold slope (FeFET, TFET…).
   1c) MOSFETs with high-mobility channel materials (III-V, Ge, 2-D crystals, CNT, graphene…) and high-K/metal gate stack.
2) Optimization of junctions and contacts to minimize source/drain series resistance and parasitics.
3) Fundamental understanding of switching mechanisms and optimization of non-charge-storage type of nonvolatile memory cells (STTRAM, ReRAM, PCRAM…).
4) Two-terminal selection devices for memory arrays. NVM cells that have built-in selection device or display characteristics that do not need selection device.
5) Revolutionary SRAM and DRAM replacement solutions.
6) Simulation/modeling of processes and devices for novel logic and memory understanding.
7) Other topics.

1a) Logic devices: Beyond CMOS devices. Use of novel materials, phases, and phenomena to demonstrate new class of computing devices

Novel logic device concepts are sought after beyond the groups 1b and 1c below. This range is wide and especially suitable for university research for novel ideas. Examples in this group are spin-base devices and Mott (metal-insulator transition) devices. It is reminded here that the research should not duplicate what is on-going in other SRC entities STARnet and NRI.

1b) Logic devices: MOSFET-like structures with steep subthreshold slope

This group of devices share the attractive feature of steep subthreshold slope beyond the fundamental limit in MOSFET principle. The device principles are different from MOSFET but the structures are similar. Particular examples in this group are TFET, based on tunneling, and FeFET (ferroelectric FET, also known as negative capacitance FET) based on ferroelectric polarization in gate oxide. Other examples are PiezoFET (piezoelectric) and IMOS (impact ionization). It is also cautioned here that the research should not duplicate what is on-going in other SRC entities STARnet and NRI.

1c) Logic devices: MOSFETs with high-mobility channel materials and high-K/metal gate stack

There have been many options being explored. Examples of materials are III-V (different versions), Si_xGe_{1-x} (different x values), graphene, CNT, 2-D crystals such as $MoSi_2$, etc. However, the demonstration of all required specifications such as on-current, off-current, low voltage, etc., have not been demonstrated. It is also important to demonstrate both *n*-channel and *p*-channel, preferably on the same material system.

2) Optimization of junctions and contacts to minimize source/drain series resistance and parasitics

It is known that in current Si MOSFETs, the intrinsic series resistance degrade the current by more than 1/3 (33%). It is expected the percentage will get worse with scaling. Means to optimize junction and contact are impactful in performance of logic devices.

3) Fundamental understanding of switching mechanisms and optimization of non-charge-storage type of nonvolatile memory cells

There are many candidates for the next main-stream two-terminal non-charge-storage type of nonvolatile memory cell. Better fundamental understand will yield improvements in reliability, multi-bit operation, scaling, and general optimization.

4) Two-terminal selection devices for memory arrays. NVM cells that have built-in selection device or display characteristics that do not need selection device

In common two-terminal nonvolatile memory cells, the low-resistance state is too conductive at low bias, leading to excessive current leakage paths in a cross-point memory array. A selection device is needed to add in series with each cell to minimize the problem. Area efficiency is an important consideration in memory cell design. Ultimately, a cell with built-in selection device in series, or a single device that displays *I-V* characteristics that do not need such selection device is the ideal solution.

5) Revolutionary SRAM and DRAM replacement solutions

Currently the continuing scaling of the 6-transistor SRAM cell and the 1T1C DRAM cell is being met with formidable challenges. Lower supply voltage, demanded by lower power, causes noise margin issues. Area scaling is another big issue. Novel device concepts to realize the same functions with fewer device components is extremely beneficial to the industry.

6) Simulation/modeling of processes and devices for novel logic and memory understanding

To help advancement in logic and memory devices, the use of numerical simulation is often required. In this area, we solicit ideas for improvements in modeling capabilities and in developing computationally efficient methods for materials, processes, and device operation. Use of these tools to study new material properties, unit processes, device behaviors, and quantum phenomena arising from nano-scale geometries is of high interest.

7) Other topics.

Outside the six focus areas above, all submissions will be considered and accepted if containing outstanding ideas.

When submitting the white papers, researchers are asked to indicate the topics (in number) what their research topic can best fit in.

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