Research Needs for Semiconductor Device Compact Modeling
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2002 Compact Modeling Task Force
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Introduction

Compact modeling of integrated semiconductor devices is one of the most critical steps in the design cycle of modern IC products. The industry's dependence on accurate and time-efficient compact models continues to grow as circuit operating frequencies increase, device tolerances scale down (with concomitant increases in chip device count), and mixed signal (analog, RF, and digital devices) content increases. Semiconductor companies, the SRC, and the Compact Modeling Council (CMC) have made significant effort during recent years to secure the future availability of high quality compact models through confidential in-house company developments and funding of North American universities. The current university program for Compact Modeling funded by SRC started in July of 2000 and will be concluded in June of 2003. SRC plans to initiate a new 3-year research program in 2003 to support university research addressing the most important needs identified in this report.

The need for better compact models becomes even more apparent in the light of recent changes and trends within the semiconductor industry. A new model for the industry is becoming established, where traditional semiconductor companies co-exist in symbiosis with foundries and stand-alone design houses. Cross-license agreements for technology IP support the standardization of transistor performance for emerging technology generations. Successful collaboration of design houses and foundries has been demonstrated with very competitive product and cost performance. Traditional semiconductor companies offer their fabrication facilities as foundries to increase the profitability of their in-house technology developments. At the same time they seek utilization of stand-alone foundries for mainstream technologies to

[1] Includes input from organizations (Agere, AMD, Cadence, IBM, Intel, Motorola, LSI, TI)

improve cost-effectiveness of products. Compact Modeling is one of the key enablers of this business model. It can certainly be called the most important vehicle for information transfer from technology fabrication to circuit and product design.

Another trend the industry is facing is the rapid approach of conventional or classical CMOS technologies to the likely end of their ability to address the most advanced 32-nm and 22-nm nodes of the ITRS. However, very promising results are reported for new directions of CMOS transistors utilizing the concepts of fully depleted SOI, Double Gate structures, and FinFETs for the 32-nm technology node and below. These new developments represent potentially a technical solution to the limitation of CMOS scaling beyond the 32-nm node. It has to be expected that the next technology generations will offer classical CMOS transistors coexisting together with non-classical devices. The development of compact models for those device structures is key to enabling successful circuit and product design. Research activities to address compact modeling of these new devices have been started, but are not nearly at the level required for successfully supporting production design cycles in the near future. Hence, a new era of fundamental research for compact modeling is necessary, which will facilitate and enable our learning curve of circuit design with non-classical devices.

A new task force was formed by the SRC during 2002 with the objective of defining a new R&D strategy for guiding future university research in compact modeling. Discussions were focused on updates for Research Needs as emerging from the trends described above. In addition, opportunities for improved infrastructure developments were discussed, serving the need of faster and more comprehensive evaluation and incorporation of new model releases into commercial circuit simulation software. The task force took notice of several very promising compiler technologies, but decided that financial support and prioritization of related research efforts related to infrastructure needs should be pursued elsewhere. The purpose of this document is therefore limited to the proposal of Research Needs and associated strategies related to further improvement of Compact Models for technologies down to the 32-nm node of the current ITRS roadmap. Areas covered include classical and non-classical CMOS transistors, bipolar and passive devices. A detailed description of the defined Research Needs is given in the next section.

The topic of this task force, “Compact Modeling” of semiconductor devices, refers to the development of models of integrated semiconductor devices for use in circuit simulations. One

aim of these models is to reproduce device terminal behavior with accuracy, computational efficiency, ease of parameter extraction, and relative model simplicity for a circuit, digital or mixed mode, or system-level simulation for the current technology node. A second aim is to provide a computational kernel capable of predictive simulation of circuits in the N+1 and N+2 technology nodes. (N refers the current ITRS 130-nm technology node, N+1 refers to the 90-nm node and N+2 refers to the 65-nm node.) The user of the model is the IC designer, and the model interface is considered as part of the model development. Physically based models are often preferred, particularly when concerned with statistical or predictive simulation.

In contrast, "device modeling", which is not the topic of this document, is concerned with the understanding and nature of detailed physical representations (often based on Drift-Diffusion models) of device operation. Device modeling is usually carried out under the umbrella of TCAD (Technology Computer Aided Design) in support of device and process design and views its audience to be principally device physicists and technologists rather than designers. It seeks to be predictive rather than being completely parameterize-able from terminal electrical measurements, and does not usually seek computational expediency or model simplicity as its chief goal. With these comments in mind, the following sections outline a description of Research Needs and their prioritization.

Definition of Research Needs

The Research Needs given in Table 1 are organized into 6 categories: (1) *Extensions BSIM4/BSIMSOI*, (2) *Next Generation CMOS Model*, (3) *Models for Non-Classical CMOS*, (4) *High-Voltage or Power Transistors*, (5) *Bipolar and HBT*, and (6) *Passives, Interconnects and Other Devices.* Explanations following describe any necessary update on the background and definition of these groups, as member companies utilized them for the voting and prioritization process.

"BSIM" is an acronym for the University of California's Berkeley Short-channel IGFET Model. The first generation BSIM model, BSIM1, became available in 1987. It was followed by BSIM2 in 1990, BSIM3 in 1994, and BSIM4 in 2000. In 1995, BSIM3 [1] was selected by all members of the Compact Model Council [2] as its standardized MOSFET model. The UC-Berkeley BSIM team released subsequent improvements of BSIM3 [3] that were co-developed with members of the Compact Model Council, though the primary BSIM research efforts were conducted under contracts from the Semiconductor Research Corporation. BSIM4 and Silicon-

On-Insulator versions of the BSIM models (BSIMSOI) are now also maintained and productized by the Compact Model Council. The BSIM models have been successfully used throughout the semiconductor industry for digital circuit design and with some success for analog, mixed-signal, and RF circuit design.

The category *Extensions BSIM4/BSIMSOI represents* the critical semiconductor industry need to continue model support for today's and future design projects utilizing single gate bulk CMOS, partially depleted SOI, and fully depleted SOI technologies. New developments for the BSIM family are expected to provide improved accuracy through the inclusion of new transistor electrical effects observed in future CMOS technologies and through improved mathematical behavior of the model equations. Furthermore, major enhancement of the computational efficiency of the BSIM family is an important research priority.

The category *Next Generation CMOS Model* addresses the industry's need to develop a new model capable of using a small number of extraction parameters to model RF performance of MOSFETs enabling the most advanced technology nodes. Although the BSIM3 and BSIM4 models have been effective for simulating circuits, they have limitations. These limitations include their being source-referenced, threshold voltage based models, and as such, having asymmetries and discontinuities in derivatives, such as capacitance and the derivative of conductance, at Vds=0. These asymmetries and discontinuities preclude modeling of distortion, e.g. IP3, for devices that swing through Vds=0. With the rising importance of CMOS used for RF applications, these inadequacies have become showstoppers for design. A next-generation MOSFET compact model is needed, that has none of the fundamental problems in present models. Models covered by the category *Next Generation CMOS Model* are expected to be fully symmetric, model all intrinsic capacitances, and pass all circuit tests. The core model is expected to be based on a small number of parameters, which are uncorrelated, greatly simplifying their extraction process. It is highly desirable that this model can be used for the extrapolation of future technologies and device parameter variation based on technology fluctuations. Such a model is critical for analog and RF CMOS simulation. Candidates for the *Next Generation CMOS Model* are expected to aim for a complete incorporation of transistor effects in future technology generations with a small number of model parameters and to demonstrate a major advancement in computational efficiency compared to models used in industry today.

Research has been started on the formulation of compact models for Double-Gate, Surround-Gate, and FinFET transistors aiming for a fully depleted operational mode. These are devices to

be included in the category of *non-classical CMOS devices*. Major changes in the material base including shifts related to strained silicon, SiGe based systems, and even non-silicon based material systems are likely to occur. Interface properties are more dominant in those devices, since the body region is fabricated using thin film technologies. The implementation of quantum mechanical carrier dynamics through the self-consistent solution of a Poisson and Schroedinger equation or any equivalent methodology is therefore a mandatory prerequisite. Although compact models in this category will be pioneers in a new field, the industry's expectations of accuracy and computational efficiency must be very high in order to enable profitable product design with technologies using those ultimately scaled CMOS devices.

Research Priorities and Funding Gaps

The Research Needs, given in Table 1, were ranked in terms of two criteria. First, the Research Needs were prioritized according to their relative importance for compact modeling down to the 32-nm node. The question asked for this prioritization is "How important is the *knowledge* and *tool implementation* obtained, related to each Research Need, to developing new compact models?" This may be referred to as the Research Priority or "Knowledge Gap", and is given in the "Priority" column of Table 1. Second, the Research Needs were ranked in terms of their funding or "Resource Gap". The question asked for this prioritization is "Given current funding in each research area remains the same, to what extent is each Research Need *adequately funded* to acquire the required knowledge when needed?" The funding includes resources provided by SRC, MARCO, federal agencies, corporate funding, etc. This ranking is referred to as the "Funding Gap" and is listed in the "Gap" column of Table 1. Both of these rankings are quite subjective, but they will guide SRC's solicitation and selection of only those highest quality proposals addressing only those topics most important to further development of compact models.

The Research Needs were ranked and color-coded into three categories of priority. The result of this ranking is represented in the "Priority" column of Table 1. Red, yellow and white colors are assigned to the high, medium, and low priority Research Needs, respectively. A definition of the color-coding is given in the "Priority Legend" below Table 1.

Prioritization of the Research Needs according to their funding or Resource Gaps is also shown in Table 1 ("Gaps" column), where the Research Needs were color-coded into three categories. A Research Need colored in red indicates *substantial additional* per annum funding

is needed to acquire the needed knowledge within the required time frame. Yellow means *moderate additional* annual funding is required, and white indicates that the per annum funding for that Research Need is adequate to obtain the needed knowledge in a timely fashion.

Conclusion: Overall Strategy for the Funding of Compact Models

The "Priority" and "Gap" ranking of Research Needs listed in Table 1 were averaged within each of its 6 categories and documented in Table 2. The color coding with red, yellow, and white background illustrates the importance of each category and the criticality of funding shortages.

Conclusions from Table 1 and 2 can be formulated as follows: (1) The *Next Generation CMOS Model* received highest results for the "Priority" and "Gap" ranking. Topics most in need of urgent attention are: *New effects, e.g. Gate Edge Drain Leakage (GED), and other new current leakage mechanisms, Specific effects of PD and FD SOI architectures,* and *Quantum effects, ultrathin oxide effects, e.g. temperature and layout dependent gate tunneling model*.(2) Next in the ranking were the *Extensions BSIM4 / BSIMSOI* and *Models for Non-Classical CMOS* category. Highest attention in the BSIM category was requested for *New effects, e.g. GEDL, and other new current leakage mechanisms.* Highest attention in the Non-Classical CMOS category was requested for *Core model for complex gate structures as in Pi-FET, DG, FinFET, etc.* and *Core model for ultra-thin body and ultra-thin gate dielectric devices utilizing full quantum mechanical modeling*.(3) The remaining 3 categories focused on the compact model development for high voltage CMOS, BJT and HBT, and passive devices were considered to be very important, but received lower overall rankings.

Finally, an overarching requirement for new compact models is that they are accurate, predictive (N+2 Technology Node) and have a relatively short execution time.

References

[1] J. H. Huang, et al., BSIM3 Manual (Version 2.0), University of California, Berkeley, March 1994.

[2] http://www.eigroup.org/cmc/

[3] http://www-device.EECS.Berkeley.EDU/~bsim3/

Table 1 –Research Needs for Semiconductor Device Compact Modeling Research Prioritization and Funding Gap Analyses

Descriptive Topic	Priority	Gap
Extensions BSIM4 / BSIMSOI		
New effects, e.g. GEDL[2], and other new current leakage mechanisms	High	High
Strained silicon, metal gate, high K dielectrics	Medium	Medium
Specific effects of partially depleted and fully depleted SOI architectures	Medium	Low
Distribution of strain and stress as function of layout.	Low	Low
Quantum effects, ultrathin oxide effects, e.g. temp. and layout dep. gate tunneling model	Low	Medium
RF: Enhanced models for intrinsic parasitics, noise, and distributed effects.	Medium	Medium
Accurate simulation of breakdown and ESD	Low	Low
Electrothermal effects, reliability, and device changes over time.	Low	Low
Noise models scalable with geometry and voltage.	Medium	Medium
Next Generation CMOS Model		
New effects, e.g. GEDL, and other new current leakage mechanisms	High	High
Strained silicon, metal gate, high K dielectrics.	Medium	Medium
Specific effects of partially depleted and fully depleted SOI architectures	High	High
Distribution of strain and stress as function of layout	Low	Medium
Quantum effects, ultrathin oxide effects, e.g. temp and layout dep. Gate tunneling model.	High	High
RF: Enhanced models for intrinsic parasitics, noise, and distributed effects.	Medium	Medium
Accurate simulation of breakdown and ESD	Low	Low
Electrothermal effects, reliability, and device changes over time.	Low	Low
Noise models scalable with geometry and voltage.	Medium	Medium
Evaluation of statistical fluctuations based on physical foundations.	Medium	Medium
Models for Non-Classical CMOS		
Core model for complex gate structures as in Pi-FET, Double Gate, FinFET, etc.	High	High
Core model for ultra-thin body and ultra-thin gate dielectric devices utilizing full quantum mechanical modeling.	High	High
Properties of high K dielectrics (frequency dispersion etc.)	Medium	Medium
Non-equilibrium thermal effects in ultrathin body devices.	Medium	Medium

[2] Gate Edge Drain Leakage (GEDL)

High-Voltage or Power Transistors

Core model for transistors with drift regions: LDMOS, DEMOS, etc.	Low	Low
Compression effects	Low	Low
Accurately accounts for drain/source diode reverse recovery	Low	Low
Accurate simulation of breakdown and ESD	Low	Low
Electrothermal effects, reliability, device changes over time.	Low	Low

Bipolar and HBT

Heterojunction effects due to large steps in bandgap	Low	Low
RF noise and distributed effects	Medium	Medium

Passives, Interconnects and Other Devices

RF models for 2,3 port inductors with complex shape	Low	Low
RF/Analog models for metal and MOS capacitors	Low	Low
Model for ferroelectric capacitor	Low	Low
Handling mask or lens imperfections leading to offsets, ACLV[3]	Low	Low
Bias dependent well resistor models that include velocity saturation effects	Low	Low
4 terminal JFET model for both junction and oxide isolated structures suitable for analog design	Low	Low
Diode model for reverse recovery	Low	Low
MEMS capacitors with novel materials	Low	Low
Efficient compact models for 3D coupled, large interconnect structures	Low	Low

Priority Legend[1]

Highest Priority Research Topic	High
Medium Priority Research Topic	Medium
Lowest Priority Research Topic	Low

Funding Gap Legend[2]

Largest Funding Gap	High
Medium Funding Gap	Medium
Smallest Funding Gap	Low

[1] There is no relative ranking. All research topics have the same priority within each color group.

[2] A critical assumption in the funding gap ranking is that current funding in these areas remains the same.

[3] Across Chip Linewidth Variation (ACLV)

Table 2 –Research Needs for Semiconductor Device Compact Modeling: Summary of Overall Rankings [3]

Descriptive Topic	Priority	Gap
Extensions BSIM4 / BSIMSOI	Medium	Medium
Next Generation CMOS Model	High	High
Models for Non-Classical CMOS	Medium	Medium
High-Voltage or Power Transistors	Low	Low
Bipolar and HBT	Low	Low
Passives, Interconnects and Other Devices	Low	Low

[3] Colors assigned as in Table 1.