FORCe II Solicitation – Research needs document

Introduction and Background:

The semiconductor industry witnessed the greatest market decline in its history in 2002 and ran into severe issues with demand and capacity management. It is becoming very clear that the coming years will witness technology acceleration as per technology analysts and International Technology Roadmap for Semiconductors (ITRS). Realizing the potential of Moore's Law requires taking full advantage of device feature size reductions, yield improvement to near 100%, wafer size increases, and manufacturing productivity improvements. This in turn requires a factory that can fully integrate the production equipment and systems needed to efficiently produce the right products in the right volumes on schedule. Preserving the decades-long trend of 30% per year reduction in cost per function also requires capturing all possible cost reduction opportunities. To continue this pace requires the vigorous pursuit of the following fundamental manufacturing attributes: maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs.

Continuation of this remarkable record now faces several challenges that threaten to slow the industry's growth, including:

1. Integrating increasingly complex factories—Rapid changes in semiconductor technologies, business requirements, and market conditions are making effective and timely factory integration to meet accelerated ramp and yield targets more difficult over time. The factory now must integrate an even larger number of new and different equipment types and software applications to meet multiple business objectives and customer requirements.

2. Production equipment performance and extendibility—Production equipment is not keeping up with Overall Equipment Efficiency (OEE) and Availability targets which has an enormous impact on capital and operating costs. The industry is unable to effectively reuse equipment or skills due to the rapid introduction of new equipment (157 nm lithography) and materials (SOI, copper, high gate stack, low dielectrics, etc.).

3. Realizing 300 mm conversion efficiencies—The industry must quickly ramp 300 mm factory production to high volumes while achieving the efficiency targets that it has set. Some of these efficiencies include >2.25 more die per wafer than 200mm, >30% cost per die reduction, 100% AMHS interbay and intrabay systems for operational flexibility and cost improvements, and the ability to track and run different recipes for each wafer within a carrier for operational flexibility.

4. Post Bulk CMOS and 450 mm wafer manufacturing paradigms—The conversion to novel devices and 450 mm wafers represent key inflection points for semiconductor manufacturing. Novel devices beyond Bulk CMOS and their potential impacts to equipment and manufacturing are not well defined, but are expected to be significant. Conversion to 450 mm wafers represents another change opportunity to improve manufacturing cost effectiveness and will be an important factor in the semiconductor industry's ability to continue realizing Moore's law.

5. Factory of the future- The challenges in data explosion (including data storage, real-time data analysis and data mining), increasing mask cost, mask reuse and technology complexity, and factory design (beyond 2007.

Key industry challenges

Dealing with these challenges means that some fundamental attributes of semiconductor manufacturing must be improved: maintaining or reducing cost per area of processed silicon, decreasing time to ramp a factory to high volume production with high yield, and increasing flexibility to adapt to new business conditions and models. In addition to incremental changes, need for Break through and disruptive technologies in factory operations is expected.

Cost per unit area of silicon and increasing cost of mask sets - Manufacturing cost per unit area of silicon is a measure of productivity. The capital cost of a factory has grown significantly each year, from $50M in the 1980s to >$2.9B in 2002. Improvements in equipment performance, continued high line and die yields, successful conversion to 300 mm wafer high volume production, continuous operating cost reductions, and cost effective incorporation of technology advancements will assure we continue this trend. Another challenge is the increasing cost of mask set (over $1M per mask set) that needs to be addressed.

Time to ramp a factory to high volume production with high yields - Decreasing time to ramp a factory to high volume production and high yield has more economic impact than reducing operating costs. (For more information on Factory Ramp, Cost, and Yield model, view the supplemental files.) New factories must be built and ramped to mature production at a much faster rate. Existing factories must be upgraded faster without impacting ongoing production.

Increasing flexibility to accommodate technology and business changes - Technology advances and the globalization of manufacturing enterprises has led to a decrease in cost for electronic components. This enables new markets to open and creates the need to increase the pace of new product introduction. The flexibility to accommodate these changes in business expectations must improve without significant cost impacts. The factories should be prepared to handle not only the technology acceleration in terms of node changes but also wafer size changes in order to keep up with the Moore's law (technology, cycle time and cost). More than ever before, factories need cost-effective solutions in a timely manner, with higher reliability and significantly reduced headcount to operate and sustain the operation, all leading to reduced wafer-cost early in the technology life-cycle. A need to handle ever exploding data, including data storage, analysis and data mining are required.

Factory operations research topics

The research topics for the factory operations research is compiled based on input from International Technology Roadmap for Semiconductor (Factory integration Section) comprising of semiconductor operations professionals from North America, Asia and Europe. Following is the list of research topics:

1. Performance improvements for simulation models for full factory with and without AMHS (inter-bay, intra-bay, and future direct transport systems) <u>for both wafer and reticle delivery in fabs</u>

2. Factory labor modeling tools appropriate for alternative labor deployment strategies under various automation conditions of: 1) No AMHS, 2) Interbay AMHS, 3) Interbay & intrabay AMHS

3. Operational control of equipment <u>and fab</u> output and cycle time variability. Including scheduling and preventative maintenance (PM).

4. Supply Chain, specific focus areas to include sourcing models, demand planning and modeling
5. Improving equipment efficiency for high mix factories
6. Backend solutions including - final wafer operations or bond, assembly, test of chips
7. Future factor design, including plug-and-play design and single wafer processing
8. Improving AMHS system throughput for interbay and intrabay
9. Financial/cost attributes in modeling (various business models, wafer cost, mask cost, etc.)
10. Factory of the future (breakthrough/disruptive technologies, single wafer processing, direct transport, etc.)
11. Innovative factory data analysis techniques including, consideration of high data volume, data analysis and data mining of factory data
12. High risk/exploratory projects in the area of factory operations addressing all the key areas (beyond 2007 needs)

Detailed factory operations research topics

Overall Area of Research	Specific Focus of Solicited Research
Performance improvements for simulation models for full factory with and without AMHS (inter-bay, intra-bay, and future direct transport systems) for both wafer and reticle delivery in fabs	Reduce model building and execution time for SIM models of full factory (7K WSPM to 25K WSPM) composed of multiple tools, multiple process/product flows and operator staffing by a factor of 50-100X reductions. Multi part number, Multi generation technology with multiple technology options. Integration of these models with factory planning/scheduling systems
Factory labor modeling tools appropriate for alternative labor deployment strategies under conditions of: 1) No AMHS, 2) Interbay AMHS, 3) Interbay & intrabay AMHS.	Develop appropriate tools for Factory Labor modeling that comprehends production floor direct and indirect tasks (including maintenance) learning rates, etc. Validate these tools using simulation modeling. Evaluate impact of Direct transport (tool to tool) on factory layout and overall design
Operational control of equipment and fab output and cycle time variability. Include scheduling and PM	Develop scheduling release, lot release; equipment set-up, batching and maintenance policies support the improvement of equipment utilization and overall factory cycle time variation (for example, adaptation of statistical methods). Improve "uptime" of semiconductor equipment by developing opportunistic planning/scheduling algorithms for PM tasks to: 1) Reduce PM duration; 2) Consolidate PMs; 3) Evaluate PM vs. Unplanned downtime tradeoffs. Evaluate e-Diagnostics, proactive monitoring of output, repair based PM, quality and variance reduction. Factory cost/ wafer cost / cycle time tradeoffs. Underlying operational scenarios, impact on fab configuration with variation in these scenarios Feasibility of Single wafer or small lot processing (improving cycle time) optimality in equipment throughput
Supply Chain: Demand planning and modeling	Develop tools, algorithms and decision support tools for forecasting demand and capacity needs. Sourcing models for volume allocation to multiple manufacturing sites. (Including supply/demand planning (matching supply to demand). supply chain collaboration, e.g. silicon foundries - fabless companies, expanding EPR & APS functionalities to handle supply networks
Equipment Efficiency	APC (Advance Process Control): Develop frame work based Fault Detection & Classification, R2R, W2W control, Integrated metrology, machine to Machine matching in order to increase yield and productivity and reduce cost; Minimize MTTR by e-Diagnostics; Equipment Engineering Systems; Equipment events integrated with factory scheduler
Backend solutions including - final wafer operations or bond, assembly, test of chips	Factory operation solutions to handle backend for scheduling, modeling and equipment productivity
Factory Design	Plug-and-play facilities systems, reduce time to factory from ground breaking; impact of automation, direct transport systems, Equipment reuse/conversion, factory information systems
Innovative factory data analysis/tools/concepts	Including, consideration of high data volume, data systems, data analysis and data mining of factory data
Factory of the future concepts	Breakthrough/disruptive technologies, single wafer processing, engineering chain, direct transport, etc. (this may be a good candidate for high risk/exploratory funding from NSF)
AMHS system throughput for interbay and intrabay	Fundamental capability that permits AMHS system to transport hot lots, gating send-ahead and hand carry. Recovery strategies after severe system failures. Impact on and requirements of transport system. Optimality of equipment and transport system reliability.
Financial/cost attributes in modeling	Develop models to comprehend standard financial attributes/metrics for factory decision making, planning & reporting. Evaluate various business models including fab-less, foundry and Integrated Device Manufacturers. Appreciation of cycle time & fab flexibility in financial terms. Also, includes, wafer cost and increasing mask cost.