Nanomanufacturing Sciences' Research Needs in Patterning, Emerging Materials, and Nanocharacterization [April 12, 2007]

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Patterning Thrust Technical Advisory Board,
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Introduction

Patterning and characterizing charge based device technologies are entering the nanomaterials era. Breakthrough advances in the basic material, chemical, and biological sciences over the last twenty years are catalyzing an explosion of novel and potentially useful materials, synthetic methods, quantitative structure property correlations, material-by-design methodologies, directed assembly technologies, and integrated approaches for nanoscale characterization. In the near future, these options may warrant consideration for fabricating advanced information processing technologies. However, material technology advances alone are not sufficient to induce changes and chemical substitution in manufacturing. In fact, manufacturing technology will change only when no other option exists.[1] Therefore, the concurrent trend in lithographic challenges is noteworthy. Recent revisions of the International Technology Roadmap for Semiconductors (ITRS) indicate that it is becoming increasingly difficult for mainstream lithographic and measurement technologies to satisfy projected ITRS dimensional scaling requirements, shown in Table 1.[2]

Year of Production	*2005*	*2008*	*2011*	*2014*	*2017*	*2020*
MPU physical gate length (nm) [after etch]	*32*	*22*	*16*	*11*	*8*	*5*
MPU gate in resist length (nm)	53	38	27	19	13	9
Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma)	3.3	2.3	1.7	1.1	0.8	0.6
Line width roughness: (nm, 3 sigma) <8% of CD	2.6	1.8	1.3	0.9	0.6	0.5
Overlay (3 sigma) (nm)	15	10	7.1	5.1	3.6	2.5

Table 1. Selected 2005 ITRS lithography variability control requirements

Current industry consensus suggests that "as the complexity of devices increases exponentially, the cost [and variability] of manufacturing also increases exponentially."[3]

Additionally, emerging application opportunities are driving the need for functional diversification, which will require enhanced functional scaling and the heterogeneous integration of new application specific materials and structures on CMOS platforms. This added complexity also challenges the extensibility of conventional fabrication and characterization methods. The convergence of these driving forces offers a rare window of opportunity for inserting novel materials, assembly, and characterization methods into nanoelectronics manufacturing. Over the next five to fifteen years, affordable nanofabrication likely will integrate the strengths and extensibility of known lithographic methods with designed high information content nanomaterials, which may exhibit electronically useful properties.

Pressure for considering innovative materials, assembly methods, and characterization tools likely will increase as the ITRS's 'red brick walls', i.e. no known solutions, continue to impact the manufacturing community's near term horizon. The convergence of these near term fabrication challenges with other system drivers, such as the market potential for emerging high margin applications, will generate and leverage a wave of novel and electronically useful nanomaterials, nanofabrication, and measurement technologies. Current manufacturing cost, complexity, and variability trends present a rare opportunity for chemists, chemical engineers, materials scientists, and others to develop breakthrough material and process insertion options that enable more favorable manufacturability, variability, and cost trends. Based on recent projections, the 22 nm ITRS technology node represents the earliest possible insertion window for innovative technologies, such as the chemical substitution of smart materials and novel assembly methods.[4]

Research Needs

Following the structure of our Strategic Plan, the research needs are divided into three categories: Patterning, Emerging Research Materials, and Nanocharacterization/ Metrology. Nevertheless, we strongly encourage research work to take a comprehensive view of technology development challenges and propose research work that bridges across areas to deliver fundamental understanding of the relationships between processing conditions, materials design, and characterization methods. We also encourage research that offers alignment and balance between experiment and foundational theory. Looking at the overall Research Needs prioritization by area, one notable outcome is the clear weighting of Emerging Research Materials topics above

other areas. However, selected topics within Patterning and Nanocharacterization also exhibit large and moderate strategic funding gaps.

Table 1-Research Needs Importance Prioritization and Funding Gap Analysis

Patterning

	Priority	Gap
Directed Self Assembly		
Nanoimprint Patterning		
Post NGL Patterning		
Manufacturing for Design		
NGL Extensibility and Limits		
Low Volume Patterning		

Emerging Research Materials

ITRS Identified Emerging Research Materials		
Application Specific Materials for Functional Diversification and Heterogeneous Integration on CMOS		
Low Temperature Processes		
Materials by Design		

Nanocharacterization and Metrology

Limits of known characterization methods		
Nanoscale defects, visual and non-visual		
Breakthrough methods, e.g. In-situ 3D imaging of atomic and nanoscale materials		
Metrology for MFD and DFM		
Measuring coupled nanoscale phenomena		
Nanoscale probe-sample measurement uncertainty		

Priority Legend[1] Funding Gap Legend[2]

High Priority Research Topic	
Medium Priority Research Topic	
Low Priority Research Topic	

Large Funding Gap	
Medium Funding Gap	
Small Funding Gap	

[1] There is no relative ranking. All research topics have the same priority within each color group.
[2] This funding gap ranking assumes that current funding in these areas remains the same.

Patterning

Directed Self Assembly

- Address Directed Self-Assembly targets to extend charge based technology

2012 ITRS Emerging Research Material Requirements: Self Assembling Materials	
Metric	**Requirements**
Defects	<0.02 20 nm defects/cm^2 [Develop a basic understanding of material and process defect related mechanisms; Develop strategies to achieve projected ITRS requirements]
Low Frequency LER	~2.1 nm 3 σ
Gate CD Control	~1.7 nm 3 σ
Resolution	11 nm
Essential shapes	Dense and Isolated L/S, circles, hexagonal arrays
Overlay and registration	5.1-7.1 nm 3 σ
Mean Throughput	1 W/Min [Via single wafer or batch processing]
Etch and pattern transfer	Satisfy projected ITRS requirements for patterning electronically useful features
Placement and orientation	20% of the critical dimension
Multiple Sizes-Pitches/Layer	2-3/layer
Ease of integration	Compatible with CMOS processing
Overall Performance	Competitive with chemically amplified resists
Other	ESH impact requirements?

Nanoimprint Patterning

- Satisfy projected ITRS overlay and defect requirements
- Electronically useful functional materials for imprint applications

Post NGL Patterning

- Develop low variability 2D and 3D patterning options that enable nanoscale and atomic scale positional control, such as for robust patterning of interfaces, gradients, and deterministic doping.

- Develop low variability patterning methods that enable direct patterning of electronically useful materials, such as nano-inkjet printing of nanometal for low temperature, high performance packaging and flash applications.
- Radical low variability patterning alternatives

Patterning/Manufacturing for Design

- Patterning/Fabrication-Design linkage and compact material/process models [Based on the outcomes of the October 2005 SRC's MFD Meets DFM Workshop. See Workshop Report.]:
  - Pattern variability minimization: The interdependence of design and patterning offers clues for addressing the emerging challenge of managing global variability. For example, new applications and architectures may help guide the choice of optimal fabrication methods. Conversely, novel fabrication processes that enable more relaxed design constraints or less process noise, such as strained silicon and other channel enhancements, may enable new opportunities in design friendly manufacturing paradigms. What materials, assembly methods, shapes, structures, and architectures can be used for laying out and fabricating high-density digital circuits that allow for maximum performance, with minimal variability?
  - Understanding critical design/manufacturing information: Design diagnostics in failure identification**:** Close the DFM loop with product test data, as opposed to unit process yield information; Link yield model to test data; On-chip test circuitry for rapid yield correlation and leakage characterization (or any performance parameter). Rapid yield learning can be achieved by having a good closed-loop system that quickly and clearly identifies design and layout issues based on real-time product test data outputs. These outputs should be in the form of binning information assimilated with proficient yield learning tools capable of distinguishing whether these issues involve wafer-to-wafer [w2w], die-to-die [d2d], or within die variations. These test data should be gathered and linked as quickly as possible into integrated design that enable performance vs. cost (yield) tradeoffs on new designs and fabrication methods to determine feasibility. Such a capability would enable new designs that exhibit optimal ramps to maximum yield.
  - Creation of integrated manufacturability models:
    - DFM-aware tools: E.g. process-aware synthesis and place and route [P&R] tools, that include timing, DFM simulators (that can estimate yield for equivalent designs)
    - Compact Models: Establish what information needs to move up and down the design/manufacturing continuum: E.g. Define an infrastructure, abstraction levels, and data models for information exchange between design and manufacturing
  - Patterning processes compatible with regular fabric architectures;
- Revolutionary options, such as:

- Patterning processes that exhibit self-healing properties and reduced process noise;
- Processes and tools that diffuse the impact of isolated defects, such as inverse/holographic mask design.

NGL Extensibility and Limits

- Novel enhancements to top down lithographic technology that enable extensions to 22 nm and beyond;
- Current research options include 193 nm immersion and EUV systems;
- Includes sources, optics, materials, models, etc.

Low Volume Patterning

- Radical concepts in low variability patterning that enable extreme scaling options

Emerging Research Materials/Nanoengineered Materials

ITRS Identified Emerging Research Materials

- Explore and assess the application potential of several families of cross-cutting materials, which include: Low dimensional materials, such as nanotube, nanowires, and quantum dots; macromolecules; directed self assembling systems; dielectrics and multiferroics; heterostructures and interfaces; and spin related materials. The research of candidate materials for specific applications is guided by the projected ITRS ERM requirements. Additionally, this sub-thrust supports the development of predictive models that enable the optimization of material performance-ESH trade-offs.

Application Specific Materials for Functional Diversification and Heterogeneous Integration on CMOS

- Explore materials and processes that enable the heterogeneous integration of complex materials on a CMOS platform and enhanced functional density. Research on these scaling independent materials would target high priority member identified enabling applications, which could include hybrid analog/digital interfaces, communication, sensing, medical systems, energy and heat management, etc. The emphasis is on robust material design for specific applications.
- The percent variability and cost of nanofabrication technology may not need to increase with each technology node. Research is needed on material and process options that exhibit potential for at least an order of magnitude reduction in fabrication variability and cost. These may include, but are not limited to: Affordable high performance materials, such as catalysts that enable the room temperature formation of complex dielectric thin films or molecular tiles that enable robust deterministic doping of channels and interfaces.
- Materials that exhibit high functional density, such as a moderate precision adder, filter, amplifier, polynomial computing block, pattern recognizer, etc.

- Materials and electronic information processing systems that mimic or are inspired by networks and dynamical systems in chemistry and biology.

Low Temperature Processes

- Room temperature catalysis and fabrication of complex composite and hetero nanomaterials, such as ceramics and other electronically useful nanomaterials
- Enable room temperature interface formation and integration with standard electronics.

Materials by Design

- Traditional empirical studies and screening methods are costly, time consuming, and inefficient. This sub-thrust will develop material structure-property correlations and predictive models for assessing and optimizing the application potential of material families, versus individual materials. This material by design capability would efficiently probe material design space and enhance the rate of progress in areas such as: Sub-32 nm resists, self-assembling materials, critical device components, interconnect and packaging materials, and other member identified application specific materials and structures.

Nanocharacterization/Metrology

Limits of Know Characterization Methods

- Future semiconductor products will be engineered at the atomic scale. This implies the need to create and develop robust atomic-scale characterization and metrology capabilities. From a device standpoint, only two pieces of data about an atom/ion are critical: its location, and its chemical identity. With these fundamental data for all atoms in a device, modeling can reveal every additional nanoscopic properties. To address this emerging need, several atomic probe methods continue development in research labs. These methods tend to be evolving towards the integration of modeling and multiple measurement techniques, which suggests the need for managing terahertz data streams and novel sampling strategies, such as analysis by exception. However, the detection of atom positions well enough to characterize mesoscopic device properties, such as stress and strain remains a significant challenge. Strain, of course, is a measure of the deviations of atomic locations from their natural equilibrium values. The following additional questions are intended to focus on the extensibility of known methods: 1) To what extent can optical methods improve information localization?; 2) Can enhanced signal to noise algorithms achieve sufficient sensitivity to quantify properties of interest?; and 3) What are some guiding principles for assessing trade-offs of existing versus new techniques?

Nanoscale Defects

- Manufacturability of high yielding nanoscale devices and circuits will require the ability to detect, characterize, and mitigate defects at nanoscale dimensions. Visual nanoscale defect detection requires rapid, real-time, non-invasive techniques that can scan large areas of 3-D structures, such as trenches, vias, and other nanolaminate and nanocrystalline structures. Of particular interest are concepts that ultimately enable automated non-destructive methods suitable for in-line, on-product monitoring of defects of sizes appropriate for a given technology generation. Corresponding characterization concepts are needed that quantify a defect's structure, position, chemical composition, and related nanoscale interactions. Non-visual defect detection and characterization, including the extensible electrical methods, will be equally important, albeit more difficult inline. Future nanoelectronic applications may require special test structures, such chemical tags or surface specific bugs that recognize specific defects[1]. Nondestructive subsurface options that probe for nanoscale defect information, identify chemical interactions, and provide 3D tomography would accelerate the knowledgebase of nanofabrication options. Additionally, the development of defect inspection sampling algorithms and mechanistically based defect models are required to handle the extremely large projected device densities and integration of new materials on CMOS.

Breakthrough Methods, e.g. In-situ dynamic 3D imaging of atomic and nanoscale materials

- The 2006 ITRS metrology chapter discusses requirements and potential solutions for emerging challenges in surface and sub-surface nanoscale characterization. There is a critical need for in-situ methods that enable robust control of material growth dynamics, interfacial structures, contacts, dopant positions and random fluctuations, catalyst design, defects, and atomic concentrations, within the projected tolerances for future device dimensions, compositions, etc. Examples of emerging nano-characterization options include: 3D dopant imaging, active dopant profiles, self-assembling material and process monitors, trace metal detection, nanostructure strain, orbital imaging, etc. Breakthroughs in nondestructive metrology and nano-characterization are needed that would enable automated and in-line measurements. Such options would provide the earliest possible feedback for development learning, process control, and ultimately reducing product scrap. Additionally, discovery research in this area will lead to new science and applications.

Metrology for Manufacturing for Design and Design for Manufacturing:

- The linkage between design, fabrication, and metrology is a critical element in the Manufacturing for Design (MFD) effort. Considerable research is needed to support ITRS projected Design Driven Metrology (DDM) requirements for globally reducing and managing process noise beyond the 32 nm technology node. Key challenges include yield metrology and characterization tools that enable improvements in long range dimensional control, line edge roughness [LER], the down stream impact of

design layout induced defect-like structures, and predictive integrated Manufacturing for Design manufacturability models. Line Edge Roughness is considered to be one of Next Generation Lithography's biggest non-tool related issue. For future nodes, its impact will increase even more. Recent simulations suggest that large gate line edge roughness (LER) significantly raises the leakage current of short-channel device, while it causing a slight increase in the drive current. This sub-thrust's success depends on the early engagement and collaboration of Tool Equipment Vendors (FAB) and EDA Software Vendors (DESIGN), especially in the design of standard interfaces and the interoperability for DFM flows.

Measuring Coupled Nanoscale Phenomena

- Research in this area is driven by the ITRS Emerging Research Device (ERD) identified potential options. Devices that may warrant characterization of coupled nanoscale phenomena include: single charge, strained, spintronic, magnetic domain, nanomechanical, etc.

Nanoscale Probe-Sample Measurement Uncertainty

- Understanding the impacts of uncertainty and transform-limited spectral line-widths on nanoscale measurements;
- Simulation necessary for overcoming uncertainties due to sample – probe interactions at the nano- and atomic scales;
- Guiding principles for an integrated atomic and nanoscale metrology strategy.

References

[1] Johannes M.C. (Hans) Stork, "Nanoscale Patterning Challenges for CMOS Density Scaling, Plenary Presentation," SPIE Advanced Lithography Symposium, 2007.

[2] Selected lithography variability control requirements, from the 2005 International Technology Roadmap for Semiconductors.

[3] Dana Blankenhorn, "Moore's Second Law Hits Home," www.danablankenhorn.com/2006/09/moores_second_l.html

[4] 2005 International Technology Roadmap for Semiconductors, *Lithography Chapter*, Figure 67. Lithography Exposure Tool Potential Solutions, 2005;