ESH/Technology Research Needs (2008 Update)

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INTRODUCTION

Investigators at the Engineering Research Center (ERC) for Environmentally Benign Semiconductor Manufacturing, as well as other investigators, will be invited to submit white papers proposing research in the area of Environmental Safety and Health (ESH) for Semiconductor Technology relevant to the members of SRC and SEMATECH. This document is a high level overview of the research topics of interest.

The submitted white papers will be evaluated by the SRC ESH Technical Advisory Board (TAB) and SEMATECH ESH Program Advisory Group (PAG) and appropriate technical representatives. A subset of the submitters will be invited to prepare detailed proposals for evaluation.

RESEARCH NEEDS

1) ESH Impact of New and Nanomaterials

This section relates primarily to current ERC Thrusts B (ESH-Friendly Novel Materials and Processes), and C (ESH Aspects of Future Nano-Scale Manufacturing).

New Materials and Associated Processes

There is an increasing demand for new and novel materials needed to continue on the semiconductor industry's classical CMOS technology roadmap, and a wide variety of additional materials will be necessary to manufacture new emerging devices beyond CMOS. Meanwhile, a more global and comprehensive chemical and manufacturing material review process based on the Precautionary Principle is being applied by governments and the public with regard to products being developed for the industrial market place (the Precautionary Principle states that**: *Scientific Uncertainty + Suspected Harm = Precautionary Action)***. In applied terms, the Precautionary Principle holds that if a new material is not comprehended from an ESH impact perspective, it should not be allowed to enter into commerce. As the industry strives for materials that have highly specialized technical performance, it must also anticipate highly protective ESH mandates for new materials. A proactive approach is needed to ensure ESH impacts are understood and goals are met while avoiding significant losses in time and investment should material and process technology developments become subject to regulatory restrictions and bans.

The purpose of material ESH research is to mitigate potential negative consequences through three focused objectives:

1. Integrate ESH performance with technology performance objectives when new material needs are identified for R&D purposes. This may include modeling techniques for predicting integrated process and product impacts, as well as identification or prediction of the inherent material ESH properties and any process by-products.

2. Develop and implement ESH methods and analysis tools intended specifically to be used during the R&D stage of material development. While fully comprehensive ESH testing methods may be inappropriate during R&D, there remains a strategic need to comprehend whether or not a given material has potential for ESH as well as technical success. The development and use of modeling tools may be important to better understand the expected behavior of new materials.

3. Establish specific research around development of environmentally benign materials, where known or anticipated new material needs can be met. Specific ESH concerns would be mitigated explicitly through development of an alternative or new material in a similar way to how technical needs are identified and met through materials R&D.

ESH for Nanotechnology

Research needs in the area of nanotechnology exist for both current and future CMOS processing and applications for 'beyond CMOS' devices. Fundamental needs applicable to both categories include:

- Definition of Nanoparticle Dose Metrics
- Application of Surface Science to Nanoparticle Characterization
- Hierarchical Risk Assessment Methods
- Nanoparticle-Bio Interaction Studies
- Predictive Materials Modeling and Statistical Data-Mining

Significant work must be done to establish the research infrastructure for nanoparticle monitoring, toxicological characterization, potential exposure pathways and bio-persistence. ESH research results and risk assessments and safe handling procedures should be shared with the nanotechnology research community.

Nano-ESH to extend CMOS

This research should focus on assessing the potential hazards and risk associated with applications such as silica and alumina nanoparticles in CMP processing, potential use of hafnium oxide nanoparticles in advanced immersion lithography, and carbon nanotubes (CNTs) that may be used in self-assembly or advanced packaging processes. Extreme CMOS options include nanowire and nanotube FETs which are being investigated in research, but may not be employed until after 2018. Nanotubes are also being explored in research for potential application to electrical interconnects. Work should be done to

establish real-time nanoparticle metrology capabilities to enable detection and monitoring of nanoparticles in air and water.

Nano-ESH for Beyond-CMOS Devices

Since many device options are available for beyond CMOS technologies the material options are broad, and most of these are currently fabricated with conventional process technologies. For new chemicals and materials to support these technologies, conventional ESH practices should be employed to evaluate and manage risk. Some of these technologies may employ nanostructured materials such as nanotubes, nanowires or quantum dots, and in some cases, free or mobile nanoparticles could be generated. While these technologies may not be integrated into products for many years, if free nanoparticles may be generated, researchers should use conservative practices to reduce potential exposure to nanoparticles until potential risks are better understood.

New Technologies for detection, hazard assessment, and toxicity screening

A key challenge associated with the rapid introduction of new materials and processes is the current lack of robust evaluation tools to rapidly assess parameters such as toxicity, materials fate and transfer, potential environmental impact. These tools fall intro three general categories: tools to measure biological activity, physical/chemical analytical methods (including metrology), and system-level tools and models for assessment of risk and overall life-cycle impacts. Additionally, chemical regulatory provisions under TSCA, REACH, and other international requirements are expected to drive information needs for both new and nanomaterials.

a) Toxicity measurement

Traditional tools for determining chemical toxicity often require significant time and expense to produce useful results. While the industry has invested significant effort to increase the availability of EHS data for new materials, significant challenges remain. With the extensive materials science research underway in the semiconductor industry, there is a need for near-concurrent screening of potential EHS impacts. Data gaps lead to over-engineering of manufacturing tools and facilities to address potential hazards. Development of reliable techniques for rapid assessment will aid in the selection of EHS-preferable alternatives.

Research is needed to apply current knowledge in biochemistry and toxicology to the creation of practical tools. While innovative approaches such as biochips with DNA attached to silicon devices to create novel sensors are currently being evaluated, substantial validation will be needed to utilize these tools in decision making. Research is needed on practical application of predictive techniques such as **quantitative structure-activity relationship** (QSAR), defined as a mathematical model that relates chemical structure to a quantitative measure of a physicochemical property or to a biological effect (e.g. a toxicological endpoint). Research is needed to evaluate if traditional QSAR analyses are valid for nanomaterials. The limited available data on nanomaterial toxicity

indicate that in addition to chemical structure, characteristics such as size, shape, surface area, clumping tendencies, and reactivity may be key factors for potential toxicity. Therefore, QSAR models that are based exclusively on chemical structure may not accurately predict toxicity or other biological effects of interest for nanomaterial assessment. Novel approaches will need to be peer reviewed and validated by appropriate organizations such as NIH and NIST.

b) Physical/Chemical Methodologies

Device research and EHS professionals are both currently challenged by limitations in analytical methodologies. Reliable analytical tools are needed to measure and characterize trace levels of materials in process effluents. Such efforts should be coordinated with the initial evaluation of materials for both advanced CMOS and novel processes. Limitations on the ability to monitor trace materials is also a major obstacle to increased recycling and re-use of ultra-pure water and process chemistries. Test and evaluation protocols will need to be validated by expert organizations like NIST.

2) ESH/Process Improvement

This section relates primarily to the current ERC Thrusts A (Novel Solutions to Existing ESH Concerns) and B (ESH-Friendly Novel Materials and Processes).

With the continued growth of the semiconductor industry and the increase in the rate and variety of new and novel chemicals being introduced into manufacturing, a focus on chemical resource management remains critical. The "Research Needs" in the process improvement area that will lead to better ESH performance revolve around five primary goals:

1) Increase in the "utilization factor" of chemicals and materials (i.e., maximizing material efficiency and minimizing waste per unit of production)
2) Reduction of the use of hazardous compounds and formation of hazardous by-products
3) Reduction of emissions of potentially hazardous compounds
4) Reduction of the "net" use of water and energy for IC manufacturing
5) Design for ESH/Life-Cycle Analysis (LCA) tools

The "Research Needs" to address these goals are discussed in the following paragraphs.

1) Chemical Utilization and Waste Reduction

The ESH section of the International Technology Roadmap for Semiconductors (ITRS) contains several references to challenges and critical needs in the area of chemical resource management, specifically related to optimization of the IC manufacturing processes for minimal chemical usage and to replacement of hazardous chemicals and materials with those that are more ESH benign. It calls for decreasing the amount of

chemicals that are used and the wastes that are produced through recycling of chemical resources, reusing of chemical resources for other purposes, and utilizing abatement options to reduce environmental releases. Although significant progress has been made in the semiconductor industry in chemical resource management, research is still needed to meet these goals in manufacturing. Ideally, better material utilization and waste mitigation should be designed into the tool and process at the development phase. However, due to the highly exacting device needs, tool design and material choice are usually optimized around technical functionality and yield, which sometimes results in utilization rates as low as 5% for some process steps. It is a real challenge for the industry to find chemicals that are more benign, less hazardous, more efficiently utilized and, at the same time, achieve the unique performance characteristics required for the advanced technologies. For this reason, novel approaches to handling process by-products and wastes are required to manage less than ideal chemicals and processes.

While there are clear ESH benefits associated with improved chemical resource management, there is also a clear business benefit. Reducing chemical consumption, using more dilute chemistries, recycling, or reusing chemicals result in cost savings and cost avoidance. In some cases, these strategies can also lead to process improvements.

Some examples of existing ESH concerns that need further attention are the amount of slurry used in CMP, the amount of UPW used for wafer rinsing, and the generation of aqueous waste containing fluoride ions, copper ions and traces of persistent organics such as PFOS. In the area of photolithography significant amounts of solvents, resists and anti-reflective coatings are wasted in their application. Further reduction in chemical usage and waste production in this area is a critical need. In the Front End processes area, new materials are being examined and developed at an accelerated rate. This is an opportunity to develop and insert Atomic Layer Deposition (ALD) precursors with a positive ESH benefit early in the adoption phase. Similarly, etch processes are being developed for the same gate stacks. An ESH friendly etch process can easily be inserted as these stacks move towards volume production.

More research is required to develop IC manufacturing that relies more on “additive” rather than “subtractive” processing, as practiced currently. This approach promises to not only reduce the number process steps (which serves to increase throughput), but also the amount of chemicals used and waste produced. This is particularly attractive in those soon-to-be adopted materials systems. A selective high-k and/or metal system that meets both manufacturing and ESH needs is seen as an opportunity.

The move to copper interconnects has made chemical mechanical planarization (CMP) an important and recurrent process step in semiconductor manufacturing that uses large quantities of water as well as consumables such as slurries, polishing pads and post-CMP cleaning brushes. The use of slurries in the actual planarization process is still very inefficient with significant amounts of the slurry by-passing the wafer. Although significant progress has been made in the understanding of the CMP process, further research is still needed to increase both the utilization efficiency of the slurry as well as to find ways to recycle the unused portion of the slurry at the tool. Ideally, one would like

to find a planarization technique that requires no slurry. More research is needed in the development of low-waste, slurry-less planarization (e.g., electro-chemical).

2) Reduction of the Use of Hazardous Chemicals

Research to identify more benign chemistries is needed in many areas. The use of perfluoro-octane sulfonate (PFOS) and perfluoro-octanic acid (PFOA) is a good example. These chemicals are used in photolithography resists, anti-reflective coatings and developers for their unique properties and performance. These materials are being considered as persistent, bio-accumulative and toxic by regulatory agencies. The industry continues to evaluate shorter-chain PFAS alternatives with improved ESH characteristics. However, there is a need for more research to develop perfluoro-alkyl sulfonate (PFAS)-free photoacid generators and anti-reflective coatings for advanced technologies. There is a need for research to find more benign dopants and implant processes. PFC emissions from etch processes are normally small compared to chamber cleans; nevertheless, with the call for further reduction of global worming gases there is a need for the development of alternatives to CF4 and low-cost, high-performance etch emissions abatement.

3. Reduction of Hazardous Emissions

There are many processes in IC manufacturing such as etch processes and dry chamber cleans that produce air emissions such as fluorine and perfluoro-compounds (PFCs), which have to be abated. Ideally, one would like to find alternative chemicals that are easier to treat or have a lower global warming potential. While great strides have been made in finding alternative processes and chemicals, there is still a need for more benign alternatives, optimization of chemical usage and less by-product formation. For example, the remote plasma chamber cleans using NF3 have markedly reduced the global warming impact, but at the same time, they produce large quantities of fluorine, which must be treated. There is a need for models to predict emissions from plasma processes. For example, many plasma processes produce hazardous by-products that are not obvious based on the feed chemical and are frequently ignored in the assessment of a chemical's environmental impact. Ideally, one would like to develop etch processes that do not use PFCs or emit PFCs. However, there are still new technologies being developed, such as through-silicon via etch (e.g., for 3D chip stacking), that use large quantities of PFCs at low utilization rates.

4) Reduction in the "Net" Water and Energy Use

For semiconductor manufacturing, research is needed into the reduction of water and energy used by wafer processing (photolithography, films, diffusion, etch and chemical mechanical planarization) and back-end (assembly and packaging) manufacturing equipment and some on-site process utilities.

Research is needed in the area of equipment design and wafer batch movement in fabs to allow implementation of a "tool idle mode" to save energy, chemicals and UPW when the equipment is not processing wafers.

For both existing and semiconductor manufacturing equipment in development, the primary research objectives should be reduction in the demand for electricity, ultra pure water (UPW), exhaust, process cooling, inert gases, vacuum and compressed air. A high priority in this area is research to optimize the energy utilization of next generation processes, and tools with particular attention to patterning equipment (e.g., there is a need for further research to develop a low-energy EUV radiation source). Other areas of interest include research into alternative process techniques that reduce the demand for laminar flow air and reduce the requirements for factory air purification and conditioning. While results from studying the higher electrical demand equipment, such as tools used in thin films, photolithography, etch, cleans, implant and diffusion, are likely to result in the greatest returns, research into increased efficiency for any equipment unique to semiconductor manufacturing, such as polishers, metrology equipment and testers, is appropriate.

For on-site utilities, the research objective is improved efficiency for systems that are unique to semiconductor manufacturing, such as ultra-pure water processing, liquid nitrogen and oxygen production, emissions abatement, waste water treatment and waste recycling. Basic research into energy reduction for facilities equipment that is common to many industries, including lighting, chillers, boilers, uninterruptible power supplies, data center equipment and monitors, will not be funded through the ERC. Research into integration of proven energy reduction concepts into existing and new factories is appropriate.

While the opportunities for chemical replacement, optimization, recycle, reuse, and abatement are many, additional examples are as follows:

- Alternative surface preparation methods (i.e., stripping, cleaning, rinsing and drying) using more benign chemicals, lower temperatures and less UPW (i.e., high efficiency wafer rinse)
- Lower hazard dopant materials
- Reduction of copper plating waste and copper slurry waste
- Recycling or reduction of consumables in the CMP process
- Etch processes that do not emit PFCs
- Low cost, high performance abatement for etch emissions
- Improvement in abatement efficiency for methanol and CF_4
- Reuse/reclaim of photoresist developer (e.g., TMAH)
- Wastewater treatment methods for new chemicals, including metals and trace compounds incorporated into devices, that end up in wastewater
- More efficient and cost-effective wastewater treatment for currently used materials (fluorides, metals, PFOS-containing materials, etc.)

5. Design for ESH/Life-Cycle Analysis

While the practical value of conducting full Life Cycle Analysis (LCA) is uncertain, the industry is recognizing the need to consider life-cycle impacts of energy and water use, material consumption, and waste products associated with semiconductor manufacturing.

However, robust databases that are readily applicable to leading edge semiconductor manufacturing are not currently available. While research is currently underway, there is a clear need for better decision-making tools that support integrating EHS criteria into process development, tool and facility design.

ESH-Related Research Needs in Semiconductor Packaging

Note: the current ERC Portfolio does not address semiconductor packaging.

Traditionally the IC package has been used to:

- physically span the die and system level geometries,
- carry signals to and from the chip,
- distribute power to chip,
- protect IC chip from the environment.

However, as silicon device technology evolves to incorporate shrinking geometries, faster switching speed, lower voltage, higher power density, Cu/low-k interconnect and biological applications, package functionality is being extended to meet heretofore unprecedented requirements such as:

- provide heat dissipation for the chip,
- provide additional interconnect layers,
- space transformation by use of 3D interconnect configurations, and
- biologically compatible packaging.

Several trends have recently impacted advanced packaging technology including 1) Pb free bump and solder ball technologies, 2) 3D stacking technologies which require substrate thinning down to below 50 um, 3) new implantable packages with bio-compatibility and 4) carbon nano-tube (CNT) -containing thermal interface materials. Research is needed to identify materials for future semiconductor packaging that are environmentally benign, operationally safe, retain functionality and reliability requirements and compliant with global ESH directives. The different materials that comprise the major components package are outlined below [The list is by no means all-inclusive, but highlights opportunities for further research].

1. Pb-free Interconnects

Bumps & Solder balls - The eutectic alloy 63Sn-37Pb, for solder balls and bumps, has generally been replaced with SnCu or SnAg alloys. Pb-free alternatives need to be identified that have thermal and electrical characteristics that exceed the performance of the eutectic alloy, while not adversely affecting device performance. Some flip chips require a combination of higher reflow temperature processing followed by low temperature lead solder attachment to the substrate. The environmental impact of rare earth alloys also needs to be investigated.

2. Encapsulation (molding) compounds

Materials used for encapsulating semiconductor devices are known as molding compounds. Molding compounds are generally composite materials consisting of epoxy

resins, phenolic hardeners, silicas, catalysts, pigments, and mold release agents. Critical properties considered when selecting a molding compound include its glass transition temperature (Tg), moisture absorption rate, flexural modulus/strength, coefficient of thermal expansion, thermal conductivity, and adhesion properties. New mold compounds should be evaluated that are recyclable, contain no suspect carcinogenic constituents like carbon black, contain benign non-halogenated flame-retardants that are not detrimental to device performance and have excellent adhesion to the lead frames. The encapsulation substances also have to be compatible with Cu and low-k dielectrics. For invasive biological applications, the bio-compatibility of encapsulation compounds requires extensive evaluation.

3. Substrates

Traditional ceramic substrates are being replaced by lower cost organic substrate that also results in a lower dielectric constant for higher-speed circuits. New organic substrates need to be identified which are more benign than the present generation of epoxy resins.

4. Underfill

Underfill materials are introduced under the devices to cover the area between the bumps, because they reduce and redistribute stresses and strains on the flip chip by forming a strong adhesive bond to the substrate. Underfill is typically comprised of epoxy formulations. Benign compounds that exhibit good adhesive and thermal cycling properties are desired in new packages.

5. Surface Cleaning

Cleaning techniques used for flip-chip assembly processes require cleaning solvents with low surface tension and viscosity to assure penetration under the die, flux contaminant solubility and residue free rinsing. The selection of suitable solvent de-fluxing chemistries requires non-ozone depletion, low toxicity and cleaning efficacy, preferably more benign than the hydrofluorocarbons currently being pursued.

6. 3D Interconnects

Identification of benign bonding agents for die-to-die, die-to-wafer and wafer-to-wafer interconnectivity as well as environmentally friendly Si etching and wafer thinning processes are required.

7. Thermal Interface Materials

Several CNT based thermal interface compounds are being evaluated for enhanced thermal conductivity applications between the die and heat spreader. The environmental impact of these materials needs careful consideration.