Introduction

Patterning and nanoengineered materials are recognized today as critical to the success of high volume device manufacturing, with enhanced functional density. It also is understood that unless metrology is considered as an integral part of the development and insertion process, then yield, performance, time to volume production, and manufacturing costs will suffer. Only by developing appropriate characterization tools can research results successfully transition to development.

University research is solicited to address the challenges which follow. These challenges have been articulated by several experts in SRC member companies and have been organized to direct interested parties to appropriate topics. While this is not an exhaustive list, it represents the priority needs of the SRC community. Researchers are encouraged to utilize industry standard tools as a basis or reference point, and to specify clearly not only how their research goes beyond the industry state of the art, but also how they would put their results into practice in an industrial setting alongside existing methodologies and tools.

In the outline on the next page, ● indicates a very important topic to a member, and ○ indicates an important topic. Also, the inputs for this outline from funding members and other interested members will be differentiated through color coding.

[Please note that a parallel effort is underway to develop a research needs document, call for white papers and proposals for SRC's ESH thrust. The ESH call for white papers is tentatively scheduled for a 1Q11 release.]

Acknowledgements

The SRC staff extends special thanks to the SRC member company representatives who contributed to this document:

Intel	Sadasivan Shankar and James S. Clarke
TEL	Benjamen Rathsack, Tsunetoshi Arikado, and Shigetoshi Hosaka
Rohm & Haas	Jim Thackeray
Novellus	Nader Shamma
NIST	Christopher L. Soles
IBM	Steven E. Steen, David Medeiros, and William D. Hinsberg
GLOBALFND	Obert Wood and An Chen
Freescale	Kevin Kemp and Willard Conley
ARO	Marc Ulrich
AMAT	Dider Florin, Christopher D. Bencher, and Kaushal K. Singh

SRC PAT/NEM/MET Solicitation for 2010/2011	AMAT	DOW	FSL	GF	IBM	INTEL*	Novellus	TEL	TI
1.0 Patterning Thrust									
1.1 Patterning Options that Enable Reduced Variability, Extensible Scaling, and Enhanced CD and Process Control	●	●	●	●	●	●	●	●	●
1.2 Directed Self-Assembly	●	●	○	●		●	●	●	○
1.3 Process Aware Compact Models, such as Directed Self-Assembly	●	○	○	○		○	●		○
1.4 NGL Extensibility / Limits	●	●	●	○	○	●	●	●	
1.5 Alternate/Non-Traditional Patterning	●	●	●	●		●	○	●	●
1.6 Nanoimprint Patterning	○	○	●			○	○		
2.0 Nanoengineered Materials									
2.1 Functional Diversification on CMOS, including materials for enabling 3D IC applications	●	●	●	○	○	●	●		●
2.2 ITRS-Identified Emerging Research Materials [CMOS and A/MS]	●	●	●	●		●	●	●	●
2.3 Process & Material TCAD		○	●	●	○	●	○		○
2.4 New CMOS and Analog/Mixed Signal Materials/Processes	●	○	●	●		●	●	●	●
2.5 Deterministic Fabrication	●	●	●			●	○	●	
3.0 Metrology									
3.1 Nanoscale Characterization and Defect Detection - Visual and Non-visual	●	○	●		●	○	●	●	
3.2 Correlate Nanostructure to Macro-scale Properties	○	○	○		●	○	●	●	
3.3 Known Characterization Methods Limits	●	●	○	●		○	●		
3.4 Metrology for MFD and DFM	●	○	●	●		○	○		
3.5 Patterning Metrology	○	○	●	○		○	○	●	

*Tentative

1. Patterning:

In 2009, the ITRS Lithography ITWG identified the following among its most difficult challenges: <2.8 nm (3σ) overlay; high sensitivity resists, with <22 nm ½ pitch resolution; low defectivity, i.e. <0.01 10 nm particles/cm^2; and <1.3 nm (3σ) line width roughness. In fact, the 2009 revision of the of the ITRS Lithography Exposure Tool Potential Solutions roadmap states the Lithography ITWG's [International Technology Working Group] consensus that there exists 'No proven optical solution beyond the 22 nm node'. However, since 2007, this Working Group also identified directed self-assembly as a potential patterning solution for the 16 nm DRAM ½ pitch node and beyond. A successful patterning technology will be cost effective and provide sufficient resolution, pattern fidelity, low variability, and throughput. This thrust seeks to find timely solutions that address these patterning challenges.

1.1 Patterning Options that Enable Reduced Variability, Extensible Scaling, and Enhanced CD and Process Control: Today's perception that manufacturing costs and percent device variability will increase exponentially with scaling is pervasive. Projected ITRS Lithography variability related requirements, i.e. for line edge roughness, long range dimensional and positional control, pattern fidelity, etc., increasingly challenge our ability to achieve advanced high volume manufacturing, with reliable system performance. Must the percent variability increase with scaling and functional complexity? Novel concepts are sought that enable extensible 2D and 3D patterning and satisfy projected nanoscale resolution, positional control, process centered and low-variability requirements. Interdisciplinary proposals are encouraged that leverage nanoscopic properties to reduce variability. This broad challenge area represents an over-arching research opportunity in patterning.

Year of production	2009	2012	2015	2018	2021	2024
MPU physical gate length (nm) [after etch]	29	22	17	13	10	7
MPU gate length in resist (nm)	47	31	22	16	11	8
Resist meets requirements for resolution and gate CD control (nm, 3σ)	3.0	2.3	1.7	1.3	1.0	0.8
Line width roughness, <8% of CD (nm, 3σ)	3.7	2.5	1.8	1.3	0.9	0.6
Overlay (nm, 3σ)	13	8.0	5.3	3.8	2.7	1.9

Table 1. Selected 2009 ITRS lithography related performance challenges.

1.2 Directed Self-Assembly [DSA]: "If DSA is to be considered a viable and competitive patterning option, it must be able to form a desired set of structures at dimensions at least a factor of two smaller than the dimensions achievable with the current optical lithography

and with twice the density as can be achieved by conventional lithographic methods. This corresponds to resolution, line edge roughness (LER), and line width roughness (LWR) targets of <12 nm, <1.3 nm, and < 1.7 nm, respectively. The structures must form in predefined locations with respect to existing structures, and with low defect density. The net time required to form and fix a pattern must be compatible with conventional inline process requirements and a throughput of one hundred twenty 300 mm wafers/hour. Also, the ability to achieve pattern registration, required feature sizes, density, low defect levels, etch resistance, and process times must be demonstrated simultaneously in an experiment with the same material." – ITRS 2009 Emerging Research Materials.

This quote reflects some of the projected DSA performance metrics that are required for this technology to be considered for insertion into a high volume manufacturing flow. The current corresponding set of directed self assembly research targets, which must be satisfied before this technology can be considered for transition to development and insertion into nanoelectronics manufacturing, is shown in Table 2. These research targets are based on the 2009 ITRS projected Lithography requirements for 2015, i.e. three to four years before DSA's earliest potential insertion date. This date was selected to reflect the need for at least three years to develop a sufficiently robust supplier infrastructure and set of patterning related products.

Tier*	Metric	Research Targets
1	Defects	≤0.01 10 nm defects cm^{-2}
1	Multiple Sizes & Pitches/Layer	≥2 sizes or pitches /layer
2	Overlay and registration	≤3.8 nm* 3 σ (2018)
2	Placement /orientation	20% of the critical dimension
2	Ease of integration	Compatible with CMOS processing
2	Etch and pattern transfer	Competitive with current resist materials
2	Overall Performance	Competitive with chemically amplified resist processing
3	Low Frequency LWR	≤1.8 nm 3 σ
3	Gate CD Control	≤1.7 nm 3 σ
3	Resolution	≤16 nm * (2018)
3	Essential shapes	Dense/isolated L/S, circles, hexagonal arrays, jogs, T-junctions
3	Effective Throughput	≥1.7 X 300 mm Wafers/Min [≥100 X 300 mm Wafers/hr]
3	Other	ESH impact, functional materials, etc.

Table 2. The current set of 2015 directed self-assembly research targets, unless noted otherwise. [Note: * Tier 1 metrics represent the areas of greatest concern, as solutions have yet to be identified. Feasibility has been demonstrated for Tier 3 metrics .]

Directed self-assembly exhibits significant traction for near term nanoelectronics patterning applications. The ITRS Lithography and Emerging Materials Working Groups lists this technology option as a potential tool for augmenting and extending current top-down lithographic processes. Candidate materials for DSA processing tend to be considered for their potential to replace photoresists, as etch barriers. Phase segregating block copolymers [BCPs], as the most mature of these materials, exhibit the nearest term insertion potential.

1.3 Computational Patterning and Process Aware Compact Models: The computational aspects of patterning and nanomanufacturing future complex systems are becoming an integral part of advanced patterning strategies. This call focuses on two aspects of this challenge: 1) Predictive patterning tools and 2) process aware patterning models for the design community. Computational lithography techniques are needed to efficiently model and rapidly explore an interdependent exposure tool, mask, material, substrate and process parameter space for specific device applications. Additionally, compact patterning models would provide designers with early access to emerging patterning technologies. This capability would ensure timely guidance for identifying optimal manufacturable and high yielding development scenarios for emerging patterning technologies, such as directed self-assembly. Computational patterning needs are driving research opportunities in the following four areas:

- Predictive patterning models that incorporate new material and process information
- Pattern variability minimization
- Understanding critical and interdependent design-manufacturing information
- Creation of integrated manufacturability models

1.4 Next Generation Lithography [NGL] Extensibility / Limits: Targeted additional research is needed on the extensibility and limits of ITRS identified and related hybrid patterning technologies. Emphasis on novel enhancements that extend the current set of manufacturable patterning capabilities, including 193 nm and EUV options, into the sub-20 nm regime may yield significant value, if it is positioned to impact identified insertion windows.

1.5 Alternate/Non-Traditional Patterning: Foundational models are needed for exploring revolutionary patterning options, such as: 1) Patterning processes that exhibit self-healing properties and reduced process noise; and 2) processes and tools that diffuse the impact of isolated defects, such as inverse/holographic mask design. This call also will consider creative approaches for patterning materials and structures for non-traditional applications. Examples of potential interest areas include, but are not limited to: Droplet-on-demand, dip-pen and polymer patterning, and directed self-assembly of gratings for waveguide, communication, health care, and energy applications.

1.6 Nanoimprint Patterning: Throughput, overlay distortions, and defects remain significant challenges that need additional research focus. The design of imprintable materials that exhibit useful and desired functionality also represents a potentially fruitful materials research area.

2. Nanoengineered Materials:

In extreme nanoscale material systems, material behavior is determined not by bulk behavior but by surfaces and interfaces. As a result, new paradigms and opportunities emerge for these new classes of materials. These include:

1. Synthesis and integration of meta, composite, and lower dimensional materials
2. Low temperature processing
3. Rapid and robust integration with CMOS
4. Functional diversification and the architecture to enable integration

The corresponding research challenges are driven by small dimensions, i.e. tens of nanometers; heterogeneous device integration; the convergence between device and material domain dimensions, and increasing interface to bulk ratios. The specific areas that need understanding are the intermediate length scales, between molecules and structures, such as grain sizes. In addition, due to the small size dimensions devices, there are many buried surfaces which need characterization. In order to address the different challenges, the following areas need focused research:

1. Modeling and metrology: Materials modeling and metrology are applied at different levels based on the accuracy and the end application requirements. There are multiple stages in which materials modeling can provide value in technology development. In the first stage during early material development, the need is to relate structure and chemistry to material properties. Since material properties determine its utility in the technology, this is a primary application of models. In the second stage, the models are applied to material improvement where they are used to optimize structure, composition, and purity. In the third stage, models are used to relate material properties to the functional properties of the device. The models at this stage in conjunction with experimental observations are used to optimize synthesis and integration. Our goals are to leverage existing thrusts and activities to address development of metrology for predicting structure and performance of devices under testing conditions.

2. Emerging Architecture: Emerging heterogeneous systems require an ability to integrate devices that are functionally diversified, i.e. sensors, power sources, converters, and super capacitors onto a silicon platform. Additionally, the potential for integrating biologically-inspired devices needs to be evaluated.

3. Low-temperature processing: Currently, most of the in-situ CMOS process flow is done at relatively temperatures, greater than 400 C. Due to the potential synthesis requirements of newer materials, which are more temperature-sensitive, novel techniques for low-temperature processing, i.e. less than 100C, and integration need to be explored.

This thrust area explores whether we can synthesize a given material, predict and measure its properties and performance, and assess its assembly and manufacturability potential. Specific examples of existing nanomaterials or material sub-systems that warrant further research include: Graphene as interconnects; CNTs as vias; integration of Graphene with CNTs; a thermoelectric converter, embedded nanobatteries, and supercapacitors integrated within CMOS; heterogeneous architectures, e.g. local 3D in a 2D architecture, high-mobility channel with conventional CMOS; structure-based design of functional materials, as meta-materials; and composite materials as dielectrics.

2.1 Functional Diversification on CMOS, including materials for enabling 3D IC applications: The 2010 ITRS is developing guidelines for projecting the requirements for systems on a silicon platform, with enhanced and complex functionality, such as tuner and demodulator chips for cell phones. Research in this area will target and address specific heterogeneous materials integration challenges for ITRS identified application areas, such as analog/mixed signal and analog/digital. Additionally, this call encourages novel material, patterning, metrology, and integration concepts that would enable extremely scaled 3D integrated circuits, as well as higher complexity and higher functionality application opportunities.

2.2 ITRS-Identified Emerging Research Materials [CMOS and A/MS]: Please see the 2009 ITRS ERM chapter for specific ITWG identified application opportunities, research requirements, and potential insertion windows.

Mat. TWG	Low Dimensional Materials	Macro-molecules	Spin Materials	Complex Metal Oxides	Hetero-structures & Interfaces	Directed Self-assembly	ESH	Metrol. & Model'g
ESH								
ERD								
FEP								
INT								
LIT								
MET								
M&S								
PIDS								

Mat. TWG	Low Dimensional Materials	Macro-molecules	Spin Materials	Complex Metal Oxides	Hetero-structures & Interfaces	Directed Self-assembly	ESH	Metrol. & Model'g
PKG								

Detailed TWG requirements or alignment | General TWG interest or alignment | No TWG interest to date

Table 3. ITRS Emerging Research Materials Matrix For Digital and Analog/Mixed Signal Applications

2.3 Process & Material TCAD: This research priority seeks to establish a rapid and robust predictive materials-by-design tool-set that reduces the time, variability, uncertainty, risk, and cost of developing and integrating new materials and processes. It would address this challenge by developing a foundational knowledge-base that enables an integrated and predictive Synthesis-Integration-Assembly-Metrology-Modeling capability to: 1) Predict functional performance, 2) synthesize new nano-material systems, 3) assemble and integrate materials to provide desired functionalities, and 4) measure a material system's performance and estimate its reliability. A key goal is to demonstrate the rapid design of new materials, from concept to prototype, in an integrated 10 nm device that is manufacturable.

2.4 New CMOS and Analog/Mixed Signal Materials/Processes: This priority area seeks novel approaches for selecting families of materials and processes that satisfy projected materials and process requirements for targeted CMOS and Analog/Mixed Signal applications. This includes low temperature and low energy processes that achieve desired process performance metrics, while minimizing resource consumption. Additional benefits from low temperature processing includes higher product selectivity and process tunability.

2.5 Deterministic Fabrication: Within the next decade, projected ITRS requirements for dimensional tolerance control will be ≤ 1 nm (3σ). Novel concepts for achieving this target are encouraged, especially if they exhibit some manufacturing potential. Atomic and nanometer scale fabrication techniques are sought that show promise for reducing statistical material and process noise and/or exhibiting novel functionality. Also encouraged are white papers that propose fundamental studies on the limits of deterministically fabricating useful materials and components on a silicon platform.

3. Metrology/Characterization:

"If you can't measure it, you can't manufacture it."
M. Postek/NIST

This interdisciplinary cross-thrust seeks creative concepts for measurement tools and methods that provide timely and appropriate characterization of emerging nanoscale materials, structures, and systems. Out of the box characterization approaches are needed to address increasing manufacturing and system complexity. It is becoming harder to accurately measure critical device and system properties as functions of nanoscopic material, process, device, interconnect, and packaging factors. For example, what combination of measurement tools would enable us to assess whether we can control, leverage and take advantage of interconnects modulated by quantum effects? The interactions between technology, integration, design, and architecture also warrant considerable study and characterization.

3.1 Nanoscale Characterization and Defect Detection - Visual and Non-visual: Research is needed to address the following gap areas –

- Atomic and Nanoscale 3D Structure and Defects, including polymers and other low-Z Materials;
- Nanoscale Probe-Sample Measurement Uncertainty;
- Nanoparticle Monitors for ES&H, which include Size, Dose, and Composition.

3.2 Correlate Nanostructure to Macro-scale Properties: The following research areas will provide new insight into nanoscopic interfaces, properties, and processes and support the materials-by-design opportunity cited in Research need 2.3, above:

- In-situ, non-destructive, 3D imaging of atomic and nanoscale materials
- In-Situ Measurements that enable enhanced synthetic and process control
- Methods that resolve and separate surface from bulk properties
- Measuring coupled nanoscale phenomena

3.3 Limits to Known Characterization Methods: This research opportunity explores and assesses the applicability and limits of known measurement methods to address emerging and projected characterization needs, such as tools that assess the dimensional variability in the domains of phase segregated block copolymers.

3.4 Metrology for MFD and DFM: This research area focuses on measurement requirements at the interface between the design and technology communities. It includes integrated measurement and modeling tools, as well as the ability to gather uniform measurements of nanoscale properties of over large areas, in a timely manner. It also encourages novel concepts for developing, processing, and integrating appropriate system on chip or self test capabilities.

3.5 Patterning Metrology: This research priority seeks novel tools and methods for addressing the Patterning measurement needs listed in section 1.0, above. For example, what combination of measurement and modeling tools will enable the characterization and correlation of a

material's stoichiometry, architecture, and 3D structure with its mesoscopic and macroscopic properties?