Packaging Needs Document

Contributors:
Ravi Mahajan (Intel Corporation), Peter Brofman (IBM), Ramakanth Alapati (Global Foundries), Claude Hilbert (AMD), Luu Nguyen (Texas Instruments), Kaoru Maekawa (TEL), Matthew Varughese (Freescale), Dan O'Connor (IBM), Sesh Ramaswami (AMAT), Jon Candelaria (SRC)

Introduction

Semiconductor based computing has revolutionized all aspects of modern life and will continue to play an influential role moving forward. In the foreseeable future computing is expected to evolve along a few broad vectors

- Small, flexible, light, easy-to-use interconnected consumer devices will continue to be broadly accepted

- Cloud based computing, that requires high compute density in Data centers and Servers, will become increasingly important

- Embedded computing that offers greater degree of control in various applications including automotive, commercial and space

In order to support the semiconductor evolution, micro-electronics packaging needs to evolve along the following directions to

- Support physical scaling of compute devices in the X, Y & Z dimensions to enable form factor and density scaling

- Facilitate power efficient, high bandwidth (wired, wireless and optical) interconnects to support increased on-package and off-package bandwidth in 2D/2.5D/3D architectures (includes memory stacks and memory + logic stacks)

- Enable high efficiency power delivery for increased battery life and lower energy costs

- Deliver cost effective thermal management. Thermal management will be a key enabler for the proliferation of 2D/2.5D/3D architectures and to ensure consumer devices meet ergonomic constraints

- Deliver reliable Materials and interfaces that will be needed to enable performance and physical scaling of packages

- Support cost effective hardware integration of sensors in computing devices

- Support heterogeneous integration in cases where System in Package (SIP) architectures are needed. Ideally there is a desire to integrate digital, analog, RF, optical and discrete devices into the high performance/low power/low cost products of the future.

- Have potential to achieve low cost implementation.

In this document we highlight the key strategic challenges facing packaging technology. For each of these challenges, the industry requires basic and fundamental understanding of the underlying science in a form that can be easily applied to developing real engineering solutions. Research project proposals specifically addressing the following science areas are welcome for consideration.

1. Global Interconnects

Packaging plays a critical role in enhancing system performance by enabling improved inter-component connectivity. The packaging challenge is to develop power efficient, high bandwidth interconnections between components. High bandwidth is provided both by enabling low loss interconnect and by increasing the number of connections between system components in a cost effective manner. There is a strong need to both develop new packaging architectures and to enhance current architectures (such as traditional organic and ceramic packaging, socket-able and surface mounted 2.5D & 3D architectures). Additionally there is a need to comprehensively model and characterize the high speed performance of the global interconnects between system components for existing and new packaging architectures. Specific areas of interest in global interconnects include:

- New packaging and system architectures, (including electrical and optical interconnects) for improved package (per socket and overall system) bandwidth + IO power efficiency. Specific targets are:

  o Data rate per line > 60 Gb/s (Electrical interconnects should target a reach of ≥ 100 mm and optical should target a reach of ≥ 30 m)

  o Power efficiency < 1 pJ/b

- In addition to improving bandwidth, research focus is needed for achieving significant improvements in bandwidth density. As interconnects push for higher and higher speeds, design requires almost full isolation of these signals from each other to avoid interference. Thus even though higher per-lane signaling rates and overall bandwidth are achieved, they don't necessarily always improve bandwidth density. Research proposals should target a linear bandwidth density > 1 Pb/(s•m).

- Electromagnetic full wave solvers capable of solving inhomogeneous, anisotropic lossy dielectrics and conductors with linear complexity for both CPU time and memory

- Validation methodologies and experimental techniques for material, component and system characterization. Specific targets are:

    o Dielectric characterization up to 300 GHz and beyond – Scope includes anisotropic and inhomogeneous materials

    o Surface roughness modeling with experimental validation up to 300 GHz

    o Rigorous de-embedding for S parameter measurements up to 300 GHz

2. Power Delivery

Future power delivery applications are expected to require transient current densities of 5-10A/mm^2 at 1V or less, and there is a need to develop solutions to meet this demand. There is also a drive to smaller form factors so the power delivery solutions should fit within the footprints of either the package or the die, and have a small z-height. Specific areas of interest for research proposals include

- Voltage regulator technologies that can support the high current densities with a relatively small footprint. The input voltage to the voltage regulator can range anywhere from 4V to 12V and the output voltage can range from 0.3V to 1V. The VR technology can be either two stage or a single stage but the overall efficiency should be in the 90+% range.

- Power delivery for electric vehicle applications – high voltage switches, regulators, etc.

- High density low impedance capacitors

    o 3D porous/trench or nanowire/nanotube capacitors targeting a capacitance density of 100µF/sq. cm.

    o Self-healing electrodes are needed for 3D capacitors

    o Leakage < $1\text{x}10^{-8}\text{A/cm}^2$

- High efficiency inductors

    o Higher resistive magnetic materials > 1miliohm-cm

    o Higher anisotropy fields while maintaining a high Bsat > 1T

- Magnetic materials that maintain their permeability at frequencies up to 1 GHz

- Integrated Batteries for consumer applications

    o Energy densities > 5x current Li ion batteries

    o Batteries must be able to withstand solder reflow conditions

- New power delivery architectures for 2D/2.5D/3D architectures.

- Wireless power delivery which is environmentally friendly for consumer applications (e.g., targeting > 80% efficiency)

Modeling and Characterization tools for new and existing power delivery architectures that enable co-design of the power delivery network with IC design.

3. Thermal Management

Reliable and affordable thermal management technology remains a major packaging challenge driven by the continuous drive towards miniaturization due to the explosion of mobile devices, and by the increase in compute density in Data Centers and Servers. There is continued interest in new and improved thermal management techniques and metrologies to address hotspots, Joule heating and overall Thermal Design Power (TDP) management in space constrained and/or high power and power density environments to ensure device performance and reliability. Specific areas of interest include

- Thermal Management Strategies for 3-D stacks, with 2 or more stacked die, that help maintain junction temperatures (T_j Memory ≤ 85°C; T_j Logic ≤ 90°C) and cover a Thermal Design Power (TDP) envelope from 2W-200W. The TDP envelope is intended to cover 2W handhelds to 200W Logic devices for High Performance Computing

- Form factor restricted thermal solutions to meet both reliability and ergonomic requirements. Passive cooling of handheld system is limited by heat rejection from the entire platform. Typical thermal solutions are expected to address both sustained and "burst" use conditions under both reliability and ergonomic requirements. (e.g., Skin temp ≤ 40°C for up to 8 hours of power on).

- Hot spot metrology and low-cost mitigation schemes including novel materials to address hot spots @ thermal densities >500W/cm^2

4. Materials and Interfaces

Advances in materials technologies, formulation methods, and process methods continue to be integral to the development of new package concepts. In addition to the novel materials and processes needed for passive integrated devices either on die or in the package, as described in Section 2, there is need for the higher dielectric constant materials, improved gap fill underfills, encapsulants, stiffer packages etc. Specific areas of interest in materials and interfaces include

- Materials for sub-20μm pitch Interconnects

    - Current carrying capability $\geq 1 \times 10^4$ A/cm2

    - Resistivity ≤ 10 μOhm-cm

    - Corrosion resistance through high temperatures up to 175°C

    - Melting point ≤ 180°C (desired to reduce the temperature-delta between room temp and m. p.)

    - Mechanical properties at least as good as SAC solder over a wide temperature window [-65°C to 150°C], i.e. modulus - 20-60 GPa, CTE ~ 20 PPM/K, Elongation > 35%, Tensile strength > 55 MPa, shear strength > 30 MPa; creep, fatigue strengths and fracture toughness [strain hardening exponents] at least equal to that of the SAC solders

- Polymeric encapsulants for 2D/2.5D/3D architectures w/ 20μm pitch Interconnects

    - Effective thermal conductivity > 10 W/m-°K,

    - Materials that allow for independent tailoring of CTE (range 5 ppm – 20ppm) & Modulus (range10-25 GPa)

    - Material viscosity that is tailorable to allow flow thru 10μm gaps

    - High adhesion strengths to silicon, metal and polymer interfaces (Si die, Cu bump, Solder bump, and organic packages

    - Glass Transition temperatures > 150°C

    - Fracture toughness [K_{1c} > 2 MPa√m]

    - Electrical insulation at < 10 μm length scales

    - Breakdown voltage one order of magnitude higher than current polymer materials, which is only between 20-30 V/um

- Material opportunities for high reliability (6-10K hours), high temperature (150-250°C), high voltage (≥ 100 V), high frequency, high density PCB technology, and low-cost automotive applications.

Focus on interfaces and identify distinguishing characteristics, including within cycling and other loading conditions. Develop methods to assess fatigue damage including test procedures and reliability models.

5. Metrologies

Metrologies that enable fundamental understanding of package performance & reliability, help improve manufacturability, and help in model validation are critical for packaging technology development. Issues of particular research interest are:

- High resolution, non-destructive metrologies for Failure Analyses that are able to resolve defects (such as TSV voids, delamination, bump, die and interface delamination cracks) at a size scale of $<1\mu m$

- Metrologies that measure package in-situ surface roughness, surface energy and mechanical properties (fracture toughness and CTE) in intricate spaces such as ~10-$15\mu m$ spaces between the neighboring interconnect bumps. Metrologies to measure surface energy & polarity with fine spatial resolution are desired. Ideally ability to measure surface energy and polarity variation across a package surface area at a spatial resolution of up ~ 2-$5\ \mu m$ or better, and surface energy accurate of ~ 1-2 dyne/cm, as a function of temperature [RT to 250 °C] and humidity [30% to 60%] at $\sim130°C$, is desired. Mechanical properties should be measurable over a wider temperature range i.e. -55°C – 250°C.

- Chemical mapping: Metrology to detect organic and organo-metallic flux residues in intricate spaces such as ~10-$15\mu m$ spaces

- Interfacial adhesion: metrology to measure adhesion strength of deeply buried interfaces across polymers-polymers, polymers-ceramics and polymers-metals as a function of temperature and humidity ranges as described above. It is especially important to characterize adhesion at the small surface areas encountered in the sub $20\mu m$ joints.

- Metrologies to measure adhesion strength of interfaces under cyclic loading.

- Board level test methodologies for packaging failures and predictive failure modeling to support rapid failure analysis and mitigation

- Packaging co-design with emphasis on enabling cost-effective, high precision/accuracy testing (to ppb levels)

6. New Concepts

Revolutionary concepts are sought to enable the electronics industry to reach new levels of integration and address emerging applications. Specific areas of interest include

- 'Stretchable' interconnects: focus on stretchable conductive materials/composites (as opposed to spring type structures where geometry enables stretching)

  - Interconnect conductivity should be as high as possible. Target value range 10000-25000 S/cm, desired envelope target: 40000-60000 S/cm (~ 10x lower than Cu)

  - The cyclical stretching ability (i.e. no plastic/permanent deformation) should be as high as possible as well. At least target 20% elastic stretch, and an envelope target of 30%.

  - Target materials to make Flexible interconnect Bend radius <5mm with <1% drain current variation for attached <2X2mm CMOS die

- Sensor packaging (MEMs & Non-MEMs) for consumer and extreme environment (e.g. automotive, oil well drilling) applications. Development of environmentally (chemical, corrosive etc.) insensitive coating materials which can be used in sensors for extreme environments.

- Concepts for low-cost, reliable, high voltage packaging (>1 kV).

- Concepts for high voltage 3D systems (PoP, stacked dies, embedding, fan-out, hybrids, etc.), including discrete FETs, passives, magnetic and sensor technology convergence.

- Materials and interface challenges involved with low-cost, high voltage, and high power packaging: Concepts for minimal silicon-package interactions (e.g., charging properties, interface conductivity) in plastic packages under humid, high temperature, and high bias that can cause high voltage device breakdown shift

- Reliability models and assessment methods for high voltage/extreme environment applications, such as downhole drilling, geothermal, heavy industrial, avionics, and automotive.

- Accelerated reliability assessment methods for automotive environments. Current automotive testing is time consuming even under aggressive acceleration factors. Need to identify acceleration factors that will reduce time

to qualification for automotive products, *and* create appropriate models which can predict field failures under aggressive including corrosive conditions.

7. Conclusion

The GRC division of SRC focuses on research in a timeframe 5-8 years ahead of technology release. This time-frame represents the "sweet spot" for pre-competitive collaborative research, after which the industry focuses on proprietary development for technology differentiation by company. Successful research proposals will need to match this timing.

This *Packaging Needs* document is not intended to be all inclusive, but rather to identify the critical areas in need of concentrated research. The GRC will host an open forum for all interested PIs soon after this Needs document is made public. Intent of this forum is to answer clarifying questions about the Needs document.

Additionally in an effort to streamline the proposal process, we encourage interested faculty to follow these guidelines:

- All research proposals should state in their introduction

  o What the state of the art is in terms of quantified capability

  o Describe how their proposal will advance the current state of the art and where possible state research targets vis-à-vis the current state of the art

  o Describe the impact of their research to system performance, reliability and manufacturability

  o A well-defined research question (or area of focus/hypothesis) with a plan for systematic analysis

- Avoid submitting proposals for

  o Areas in that are already in development or deployment unless the specific research question is clearly shown to be strategic and can be generalized beyond current applications

  o Analyses projects that don't involve modeling methodology improvements that will significantly improve modeling capability

  o Materials characterization projects that don't involve characterization method improvements or where results cannot be broadly generalized

  o Compact Models