Memory, Logic, and Logic in Memory Using Three Terminal Magnetic Tunnel Junctions Massachusetts Institute of Technology 77 Massachusetts Ave, Cambridge, MA, 02139

# E2CDA-NRI Year One Semi-Annual Report

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### Luqiao Liu, Massachusetts Institute of Technology

#### **Executive Summary**

The main focus of our center is to develop magnetic switching device and circuit for overcoming the increasing gap between the performance of processor and memory in speed and power consumption. Currently systems dissipate huge amount of power making up for this gap with support logic such as caches, which result in further power consumption and extra CPU landscape. We are trying to exploit the dual capabilities of magnetic tunnel junctions in logic and memory devices to address the issues mentioned above.

Two themes are pursued in our center to address the memory wall issue: first, we are optimizing materials and device structure of magnetic tunnel junctions which will increase the speed and lower energy consumption of non-volatile memories to the same level of main stream cache memory. Second, 'logic in memory' architecture is studied using magnetic tunnel junctions to perform logic within memory arrays.

In the past 6 months, we have made progress in tasks under both themes. First of all, for magnetic switching device and material development, we achieved (1) spin orbit torque induced switching in nearly compensated ferrimagnet electrode. Along this direction, we modified our original proposed approach of using synthetic antiferromagnetic multilayers (such as [Co/Tb]n for switching device. Instead, we used the compensated ferrimagnetic alloy. The advantage of ferrimagnetic alloy over multilayer is that it allows better control over the net magnetization as well as stronger perpendicular anisotropy. The usage of ferrimagnetic alloy is a Cobalt terbium alloy was utilized and the spin orbit torque switching efficiency was quantified in a series of samples. It turns out that the spin orbit torque gets to the maximum value in nearly compensated samples, which makes it a very promising candidate for magnetic free layers in memory or memory in logic device. The fast switching speed expected in this type of material could pave the road towards sub-ns switching speed and sub-pJ switching energy devices. (2) Development of low moment ferrimagnet insulator and characterization of their properties. The motivation for us to study ferrimagnetic insulator is that devices that incorporate magnetic insulators to isolate the input channel and the output channel will maximize spin orbit torque efficiency and allow for general purpose spin based non-volatile logic. In our initial period, two different type of ferrimagnetic insulator films were developed. Their structural and magnetic properties were characterized. For initial experimental testing, the spin Hall magnetoresistance was employed as the readout method. In the final realization of these devices, the magnetic insulator will be incorporated into magnetic tunnel junctions and TMR will be employed as the reading method. The second theme of our center task of is to use three terminal MTJs to perform logic within memory arrays. In the past 6 months, we have obtained the following results: (1) determining the appropriate bit precision that provides a good trade-off between accuracy, cost and feasibility to be implemented in MTJ, and (2) understanding the domain wall behavior for domain wall motion based logic in memory devices. The goal of these two activities is to get better understanding on using MTJ as multibit resistor and non-linear threshold device, which will finally allow for the integration of magnetic switching device into a convolutional neural network for cognitive computing.

As is mentioned above, in this initial period of award, we have made progress in areas of material development, physics mechanism study, device fabrication, simulation and circuit modelling. The understandings gained on material, device and circuit level will facilitate our efforts in the following development of memory and logic in memory device and circuits.

# Theme 1: Low energy three terminal magnetic switching device (Luqiao Liu, Caroline Ross and Marc Baldo)

### **Theme Executive Summary**

In the past half of the year, the main focus of theme 1 is to develop materials and physics mechanisms that could be utilized to realize fast and low energy magnetic switching device, which is the key prerequisite for realizing logic-in-memory architectures. Particularly, we have made great progress in two sub-tasks: (1) demonstration of spin orbit torque induced switching in nearly compensated ferrimagnet electrode. This paves the road towards sub-ps magnetic switching and low power memory device (with switching energy lower than 100fJ). (2) Development of low moment ferrimagnet insulator and characterization of their properties. Magnetic insulator can couple metallic layers magnetically while isolate them electrically in domain wall based logic-in-memory devices, which can greatly reduce the current dissipation inside ferromagnetic metal layers and allow for ultra-efficient magnetic switching device.

### Task 1: Spin orbit torque switching of zero moment magnet (Lugiao Liu and Marc Baldo)

Despite the potential advantages of information storage in antiferromagnetically coupled materials, it remains unclear whether one can control the magnetic moment orientation efficiently because of the cancelled magnetic moment. In this period of the award, Liu and Baldo focus on spin-orbit torque induced magnetization switching of ferrimagnetic  $Co_{1-x}Tb_x$  films with perpendicular magnetic anisotropy. Current induced switching is demonstrated in all of the studied film compositions, including those near the magnetization compensation point. The spin-orbit torque induced effective field is further quantified in the domain wall motion regime. A divergent behavior that scales with the inverse of

magnetic moment is confirmed close to the compensation point, which is consistent with angular momentum conservation (see Figure 1). Another experimental observation from these experiments is that while the saturation magnetization Ms decreases, the coercive field increases as 1/Ms, which guarantees that the total anisotropy energy coefficient  $K_u \sim M_s H_c$ remains finite and satisfied the requirement on thermal stability. The demonstrated spinorbit torque switching, in combination with



Figure 1: Magnetization curve of nearly compensated CoTb alloy film (left) and current induced magnetic switching as is detected in Ta/CoTb bilayer film.

the fast magnetic dynamics and minimal net magnetization of ferrimagnetic alloys, promises memory and logic in memory devices that are faster and with higher density than traditional ferromagnetic systems. The switching speed of compensated ferrimagnet is under investigation via the current induced domain wall motion approach. The experimental observation of SOT switching of compensated ferrimagnet can have influence in the following two areas for the development of spintronic memory or spin logic device: 1) the developed low Ms or zero Ms material will not only work for spin orbit torque switching but also conventional spin transfer torque switching. The technology can be easily transferred onto STT-MRAM system and gets fast switching. 2) spin orbit torque materials which can generate out of plan non-equilibrium spins have recently been identified. It is believed that the utilization of these materials will allow for anti-damping switching on the compensated ferrimagnet and ensures low writing bit error rate.

### Task 2: Development of compensated ferrimagnet insulator (Caroline Ross)

During the initial period of the award, Ross worked on developing new ferrimagnetic insulators for spin orbit torque experiments. Prior work focussed on thulium iron garnet, TmIG ( $Tm_3Fe_5O_{12}$ ) which we chose because we expected it to show perpendicular magnetic anisotropy due to its epitaxial growth on a single crystal GGG ( $Gd_3Ga_5O_{12}$  garnet) substrate. This led to a magnetoelastic anisotropy sufficient to

overcome shape anisotropy and yield PMA, at least in the (111) orientation. TmIG/Pt showed spin orbit torque switching in which the TmIG magnetization could be reversed by applying a current in the Pt (Avci et al., Nature Materials 2016). Our recent work included growth of two new garnets, EuIG and TbIG. The TbIG has a compensation point which will enable SOT measurements analogous to L. Liu's recent work on ferrimagnetic



Figure 2: Xray diffraction of a TbIG film on (111) GGG, showing high quality epitaxial growth and a perpendicular magnetic anisotropy (measured by magnetooptical Kerr effect).

conductors (Finley et al.). EuIG is expected to have PMA in both (100) and (111) oriented films which may enable PMA in polycrystalline films for purposes of integration on Si.

We carried out a major overhaul of our pulsed laser deposition system, increasing the intensity of the laser which has improved the growth of the films. We synthesized EuIG and TbIG targets and deposited films of TbIG. The TbIG showed very good film quality and epitaxy, with PMA as expected (Figure 2). The films are much smoother than previous films without second phase particles which suggests a better stoichiometry control. The next steps will be to examine SOT in Pt/TbIG bilayers.

### **Journal Publications**

### **Conference Publications**

• Spin-Orbit Torque Efficiency in Compensated Ferrimagnetic Cobalt-Terbium Alloys, Joe Finley, Luqiao Liu, Annual Conference of American Physical Society, March, 2017

### **Students this Period**

Joseph Finley

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### Theme 2: Logic in Memory (Vivienne Sze, Marc Baldo and Caroline Ross)

### **Theme Executive Summary**

Modern processors dissipate at least 100× more energy when reading memory than performing simple arithmetic. The dual capabilities of spintronics in logic and memory will be used to address the 'memory wall' by incorporating logical functions directly within memory in order to reduce this costly data movement. The goal of this theme is to use Magnetic Tunnel Junctions (MTJ) to perform computations commonly found in deep convolutional neural networks. This includes using the MTJ as a variable resistors to perform a multiply and accumulate, and using the MTJ with a variable channel width to perform the non-linear function. In the past 6 months, our efforts in this theme focus on (1) determining the appropriate bit precision that provides a good trade-off between accuracy, cost and feasibility to be implemented in MTJ and (2) understanding the domain wall behavior for domain wall motion based logic in memory devices.

## Task 1: Analysis of the impact of Bit Precision of MTJ on neural networks performance(Vivienne Sze):

The bit precision of computation using MTJ can be limited due to the cost and variations in fabrications. At the same time, bit precision affects the performance accuracy of deep convolutional neural networks. In this task, we examine the impact of reducing the bit width on accuracy for a task such as image classification. We will also compare the impact of bit width on MTJ versus conventional digital CMOS in order to quantify the benefits in terms of energy and area. Due to the extended negotiation on the IP terms between our institute and SRC, the funding on this task only arrives about a month ago. A graduate research assistant was recently hired and started to work on this topic.

## Task 2: Study on the domain wall motion behavior for logic in memory devices (Marc Baldo and Caroline Ross)

In our proposal of using domain wall MTJ device for neural networks, when the wire width is scaled to below 100 nm, effects from wire edge roughness

increasingly dominate the operation of these devices. Ross and Baldo completed experimental and computational work on domain wall behavior in very narrow magnetic wires, where the line edge roughness leads to pinning that limits the locations where a domain wall is stable. We developed an analytical model for the distribution of domain walls into discrete positions under steady-state applied magnetic fields, basing our model in part on the edge deviation fractal model. We found good agreement between the analytical model and measurements on Co wires in micromagnetic simulation and in experiment. These results are relevant to domain wall device applications as they are scaled into regimes where line edge roughness dominates the nanowire energy landscape.



Figure 3: Magnetic force micrograph of magnetic domain walls in concentric nanowire rings, where individual nanowires are simulated in realistic micromagnetic models.

### Journal Publications

 The Spatial Resolution Limit for Domain Walls in Sub-100-nm-wide Magnetic Nanowires, Sumit Dutta, Saima A. Siddiqui, Jean Anne Currivan-Incorvia, Caroline A. Ross, and Marc A. Baldo, submitted, 2017

### **Conference Publications**

- Energy-Efficient Hardware for Deep Convolutional Neural Networks, Vivienne Sze, SRC eWorkshop, Jan 10<sup>th</sup>, 2017
- The Spatial Resolution Limit for Domain Walls in Sub-100-nm-wide Magnetic Nanowires, Sumit Dutta, • Saima A. Siddiqui, Jean Anne Currivan-Incorvia, Caroline A. Ross, and Marc A. Baldo, Annual Meeting of American Physical society, March, 2017
- The Analog Information Limit of Magnetic Domain Wall Positions in Nanowires, Sumit Dutta, Saima • A. Siddiqui, Joseph T. Finley, Caroline A. Ross, and Marc A. Baldo, MRS Spring Meeting, April 2017

## <u>Students this Period</u> Sumit Dutta

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started graduate student

# Journal Publications, Conference Presentations, Patents and Disclosures for this Reporting Period

### <u>Totals</u>

Contribution type	Number of New Contributions
Journal articles	1
Conference papers/presentation	4
Patents & Disclosures	0

### Journal Publications

• The Spatial Resolution Limit for Domain Walls in Sub-100-nm-wide Magnetic Nanowires, *Sumit Dutta, Saima A. Siddiqui, Jean Anne Currivan-Incorvia, Caroline A. Ross, and Marc A. Baldo, submitted, 2017* 

### **Conference Publications**

- Spin-Orbit Torque Efficiency in Compensated Ferrimagnetic Cobalt-Terbium Alloys, Joe Finley, Luqiao Liu, Annual Conference of American Physical Society, March, 2017
- Energy-Efficient Hardware for Deep Convolutional Neural Networks, Vivienne Sze, SRC eWorkshop, Jan 10<sup>th</sup>, 2017
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### Patents and Disclosures

### **Students this Reporting Period**

### **Student Name**

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Sumit Dutta Joseph Finley sumitd@mit.edu joetfinley@gmail.com Status Whereabouts (new, post doc, graduated) started graduate student started graduate student