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Nanoelectronics RESEARCH INITIATIVE

NRI Feedback SWAN

SWAN Review
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Feedback SWAN Center Overall

- Overall vision/content of center and fit into NRI mission?
  - SWAN continues to be a very good example of what NRI strives for: a center that effectively integrates basic science research with engineering to try to translate that science into devices
- Center organization & operation?
  - Sanjay does a very good job of organizing the center technically, to maintain a focus on the overall mission
    - Also very good at integrating the assignees into the work effectively
  - The center has grown well over the past 5 years, and is much better organized and focused than it was originally
    - Maintains a strong physics theory core, but has integrated that well with the device and processing work necessary to demonstrate that theory
  - Review was well organized and gave a clear picture of the work overall
    - Nice linkage between the talks and posters
    - Appreciate the explicit reference to the previous year's feedback – clearly tried to respond to that in their work over the past year
- Feedback on overall progress / results thus far?
  - Center has really come a long way – developing into a true "center" versus a collection of projects
  - Progress on most aspects of the devices and theory have been very good; continue to focus on how best to get experimental evidence to support the theory work as quickly as possible

Feedback SWAN Center Overall

- Areas to emphasize for Phase 1.5?
  - Maintain strong focus on the BiSFET – and be sure there is enough effort on it: must get enough data to prove out the key parts.
    - Build a plan to be sure this happens: What structures are needed? What are the key process modules that need to be developed? What characterization is needed? What further modeling or theory work is needed to understand intermediate results? Can industry help more?
  - Extending into other collective or single particle tunneling structures is reasonable, but maintain a focus on unique applications of this, beyond standard TFETs
    - HetTFET work is potentially viable, but must be in sync with MIND
      - Must show that the issues that impacted many TFETs in MIND (and elsewhere), including phonons, Dit, etc., won't also diminish the performance here; Must have a experimental plan in mind
  - The addition of other devices should be guided by whether they have strong synergy with the core BiSFET/graphene work
    - The topological insulator version of the BiSFET device seems like a well-related option – coordinate with FENA
    - The exciton FET (Appenzeller) may also be a good addition
    - Don't try to add entirely new devices at this stage – those are more appropriate for the NRI-NSF NIRT awards
  - Continue to look at circuit and architecture issues in parallel, taking into account new data as it comes from the device experiments
- Interaction with industry / government partners?
  - SWAN has been very open with the assignees and very willing to have them be an integral part of their research
  - As was stated in last year's feedback as well: Can industry/NIST labs help you fabricate parts of the devices to accelerate experimental verification?
- General comments
  - Materials learning for graphene devices is valuable, even if BiSFET itself doesn't work
    - More work on patenting some of these key ideas would be useful – IP is valuable, in addition to publications
    - Consider patenting not just process / technology, but also circuits / architecture

Feedback SWAN Projects

- Pseudospintronics; Graphene
  Tutuc, MacDonald, Sinova and Register (UTA); Hwang/DasSarma (UMD)
  - Tutuc: Experimental work on creating bi-layers / BiSFET
    - Very good experimental work on trying to fabricate and characterize the BiSFET structure
      - Continue to work to add the top gate – it would be good to see a clear roadmap of the stages they have planned for building and demo'ing the devices
    - Needs even more activity in phase 1.5 to ramp up effort on the BiSFET – add a post-doc? Tutuc is doing a good job directing the students, but may need more bandwidth than he can supply alone
  - Tutuc: Spin injection into Ge nanowires
    - Interesting results, and nice work verifying spin injection through remote sensing
    - Given that the signal level continues to be very small, agree with decision to focus on the BiSFET instead for Phase 1.5
  - MacDonald: Continuing work on "RT" coupled-2D systems (graphene and now TI's)
    - Appreciate the efforts to continue to refine the theory for graphene condensates, including new effects, as well as expanding into related areas such as topological insulators
      - Focus the effort on understanding how to prove this theory is accurate – more important than refuting other people's theories (there will always be competing theories)
    - Build a joint roadmap of how experimental results can build-up to prove this theory: what does Coulomb drag tell us, e.g.? Give guidance of what experiments need to be done next.
      - Given the current structures, should the condensate have been seen already at low temperatures? Or what is limiting it? What is the "simplest, realistic" structure that could be built that would show it at low temperatures?
  - MacDonald/Sinova: Spin intrinsic Hall Effect (SiHE) work
    - Showed very good results in terms of demonstrating that SiHE can be detected electrically and showing how individual logic gates could function – the right combination of work for NRI
    - However, we agree that the large mismatch between input and output signals makes it an unlikely candidate for sequential logic to be pursued in Phase 1.5

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- Pseudospintronics; Graphene
  Tutuc, MacDonald, Sinova and Register (UTA); Hwang/DasSarma (UMD)
  - Huang/DasSarma: Transport in graphene
    - Presentation was a bit hard to follow, but the work on disorder and puddles is very important – really helps us interpret the results being measured on our current (disordered) material, to separate the real physics from the artifacts
      - Interesting results showing the impact of these puddles on both resistivity behavior with temperature and bandgap measurements
    - Continue to focus on how these effects are affecting the specific structures being pursued for devices in SWAN (BiSFET in particular)
      - Really appreciated the insights into the effect of phonon and plasmon coupling from the substrate, and hence the importance of choosing the right substrate for devices
      - Other areas to potentially consider: What are the effects of some of the specific problems we're seeing in our material now: the wrinkles, the strain, etc.? How "puddle-free" could we ever hope to be in a graphene mono- or bi-layer, and how does that affect our ability to get a condensate?
  - Register: Achieving, optimizing, and controlling the condensate for devices
    - Good work trying to understand the parameter space and where we need to be in it (realistically) to see the desired results
      - Good progression from mapping out the basic parameters (epsilon, thickness, carrier concentration, etc.) and now expanding into the less obvious (effect over larger areas of rotation, disorder, amorphous dielectric, time dependence for condensate breakdown, etc.)
    - Consider also how to build models that help us understand the intermediate stages before we get the ultimate structure
      - E.g. understanding the connection between Coulomb drag and a condensate; understanding what we need to see the condensate at low temperature at least; etc.
    - At the circuit/device level, would be good to try to estimate the parasitics and clock energy as these models develop

Feedback SWAN Projects

- Characterization and Modeling of Materials and Processes for Graphene-based Devices
  Vogel and UTD team; Ruoff (UTA)
  - Really appreciate how this work has coalesced over time to support the device efforts significantly
    - The work on unit processes for various components is very good; make sure there is also strong collaboration between UTD and UTA on the overall device flow, integration, materials work, and characterization – specifically to produce a BiSFET demo
  - Consider putting together the full process flow needed for a BiSFET demo, with a list of key challenges for each step – the simple 5-mask flow for processing large area graphene into devices shown by Vogel is a good start
    - Farm out work to various teams to work on each challenge
    - Is there anything more industry / NIST can do to help on any of them?
  - Vogel: Metal contacts and Graphene on Cu characterization
    - Good to see the systematic work to understand the confusing data coming from the contacts right now – e.g. the edge effects – very important to graphene research overall
    - Appreciated the comparison to the mobility measured at Columbia – important to keep this kind of cross-university work going, to make sure we are seeing a consistent picture
    - Showing how much spread there really is in data right now (mobility, contact resistance, etc.) was very important – helps us understand the uncertainties involved
  - Wallace: XPS on ALD Al_2O_3 Dielectrics on graphene
    J. Kim: ALD dielectrics on graphene
    - Important learning for building a device – make sure it is picked-up rapidly for the device fab process flow (at UTD and UTA)
      - Nice linkage between the Kim and Wallace groups on this work
    - Finding ways to "attach" the dielectric without disturbing the surface is important: Does a chemical bond destroy the graphene?
      - Should we be thinking about how to attach a dielectric (by VdW forces maybe?) to a monolayer, rather than our traditional approach to attaching it to a surface?

Feedback SWAN Projects

- Characterization and Modeling of Materials and Processes for Graphene-based Devices *Vogel and UTD team; Ruoff (UTA)*
  - M. Acik/Chabal: Thermally-derived Graphene
    - Interesting materials work, and appreciate the thorough analysis of the material
      - Would be good to include transport measurements as well
    - Not really clear where this fits into the overall device work – it doesn't seem like a path to producing high-quality graphene, but could be important learning for other approaches
      - Be sure this is focused on learning about graphene and surface/chemical interactions to help the main device efforts
      - Could graphene oxide be a dielectric for a device?
  - Floresca/M. Kim: Microscopy on graphene
    - Very good set of imaging techniques, and some impressive images on graphene and BiSFET structures
      - Would have been good to see more discussion on how these results impact the device fabrication or characterization directions
    - Would be interesting to compare the exfoliated and CVD-grown graphene quality – exfoliated graphene may also have unexpected defects
  - KJ Cho: Graphene Materials Theory
    - Understanding the fundamental theory behind the key materials/structures is important
    - Seems to be well-synced to experimental work – the structures being modeled (metal/graphene contacts, grain boundaries, growth on an inert surface) seem to match the current big questions from the device side, so keep that connection strong
  - Ruoff: Growth and Mobility
    - High quality graphene is key to all the work, so this project is fundamental
      - Good interaction with UTD for the characterization of mobility and other properties
      - Appreciate the continued work to get higher quality, larger areas, larger domains
    - Finding ways to grow on more relevant / integrable substrates (e.g. BN or other dielectrics) is important if it is possible – avoiding transfer off of Cu would be very useful
      - Also appreciate work on adding Ni to try to controllably grow multi-layer graphene

Feedback SWAN Projects

- Nanoscale Heat Management: *Pop (UIUC), Kim (NCSU)*
  - Overall, this continues to be seen as a useful area of research for NRI; for Phase 1.5, the challenge is to focus it on the specific devices vs. the general problem of heat management / cooling
    - Can we build a thermal model / experimental structure for thermal flow in the BiSFET? Are phonons likely to be a limiter for condensate formation, and if so, how can we choose materials / structures that mitigate that interaction? How do we model and manage nanoscale phonon flow?
  - Could also help us learn more about carrier flow in general
    - Could looking at 2D maps of breakdown or thermal flux help us understand where current is flowing in graphene (near the edges)?
  - Pop: Thermal Flow across Interfaces in CNTs/Graphene
    - Very interesting results on how CNTs and graphene couple to a substrate for thermal conduction – important to a variety of devices
    - Really like the combination of thorough experimental work with high-level modeling to understand the results – encourage also coupling the work more closely to the advanced modeling being done by Kim
    - Also appreciate the collateral findings, such as a methodology for counting 1-10 graphene layers
  - Kim: Nanoscale phonon flow modeling
    - The first principles modeling of phonon dispersion in these materials is very important for understanding how it can impact devices – be sure to maintain a strong linkage to the specific materials/structures/devices being pursued, and use this actively when making decisions on which m/s/d should be pursued (e.g. BN substrates)
- NanoMagnetic Logic: *Varga/Porod (ND)*
  - The slanted supermalloy nanomagnets look interesting for producing AND/OR logic directly
    - Good example of work on finding new approaches to architecture to reduce logic footprint – although scaling a patterned magnet shape to small dimensions may be challenging
  - Overall, NML work continues to be of interest, and will be pursued in MIND/WIN
- Novel Plasmonic Interconnects: *Massoud (Rice)*
  - Plasmonics in general still look most promising for interconnects only, not logic devices, so agree this fits better in IFC or another venue