SRC India Research Program: Research Needs
March 2020

The Semiconductor Research Corporation (SRC) India Research Program (IRP) member companies are pleased to release this document that describes the 2020 research needs.

The India Research Program research needs of the members are described in two major categories:

- Tools, Flows, and Methods
- Architectures and Circuits

Each of these major categories are broken down into several sub-categories which describe the need in more detail. Even so, these are written to be broad in nature to not restrict the investigator's approach. There is no priority assigned to the order of either the major categories or the sub-categories.

This needs document is driving the India Research Program solicitation. It is issued to universities throughout India, may be addressed by an individual investigator or a research team. Our selection process is divided into two stages. The interested party is requested to submit a brief 1-page white paper. The white paper should clearly identify what can be done in three years. A successfully selected white paper will result in an invitation to submit a full proposal. These proposals will be further down-selected for SRC research contracts.

Investigators who are funded will be expected to publish at top-tier conferences, including but not limited to ISSCC, VLSI, HPC, ISCA (part of Federated Computing Research Conference), and ESWEEK (CASES, CODESISSS, & EMSOFT).

White Papers for all the categories below will be considered for funding. Investigators are limited to participation in two white papers in this IRP solicitation. Submissions should highlight major category needs are addressed, such as "I1".

CONTRIBUTORS

ADI	Aravind Navada
IBM	Arun Joseph, Rahul Rao
Intel	Anand Ananthanarayanan, Sreenivas Subramoney
NXP	Sourav Roy
TI	Rubin Parekhji

2020 India Research Program Needs Categories	
I1	**Tools, Flows, and Methods**
I1.1	Design for robustness: tools, techniques, architectures, and systems
I1.2	Test techniques: yield learning, RF, mm-wave, high-speed, high-level, diagnosis, and repair, approximate test, big data analysis, analog BIST, defect coverage driven alternate / structural tests, and fast methods for analog fault simulation
I1.3	Design verification and validation techniques: core algorithms, formal approaches, model generation, analog/mixed-signal, mm-wave, post-silicon, system-level, and security. ML methods
I1.4	Design for safety and safety mechanisms, and safety analysis techniques
I1.5	Design optimization for functions including power management, energy harvesting, clocking, and RF baseband
I1.6	Compact circuit simulation models for analog/mixed-signal devices
I1.7	System level design optimization, including early exploration with SW/HW co-development for multi-core SoC designs, and energy efficiency
I1.8	Design for security of information systems, embedded systems and automotive systems, including accelerators and HW/SW co-design
I2	**Architectures and Circuits**
I2.1	AI, cognitive, machine learning, and deep learning: architectures, techniques and applications for IoT edge devices to the cloud
I2.2	Cloud computing, analytics: enabling architectures, techniques, and applications
I2.3	Architectures, accelerators, reconfigurable computing, hardware-software co-optimizations for cognitive computing, machine/deep learning, computer vision, FMCW radar and LIDAR.
I2.4	Architectures for near-memory and in-memory computing using both traditional memories and emerging non-volatile memories
I2.5	Cache and memory hierarchies for general-purpose and domain-specific systems
I2.6	Security and safety of analog signal chains