SRC Microelectronics Manufacturing USA Institute Informational Webinar

# Advanced Microelectronic Packaging for Energy Efficiency Scaling

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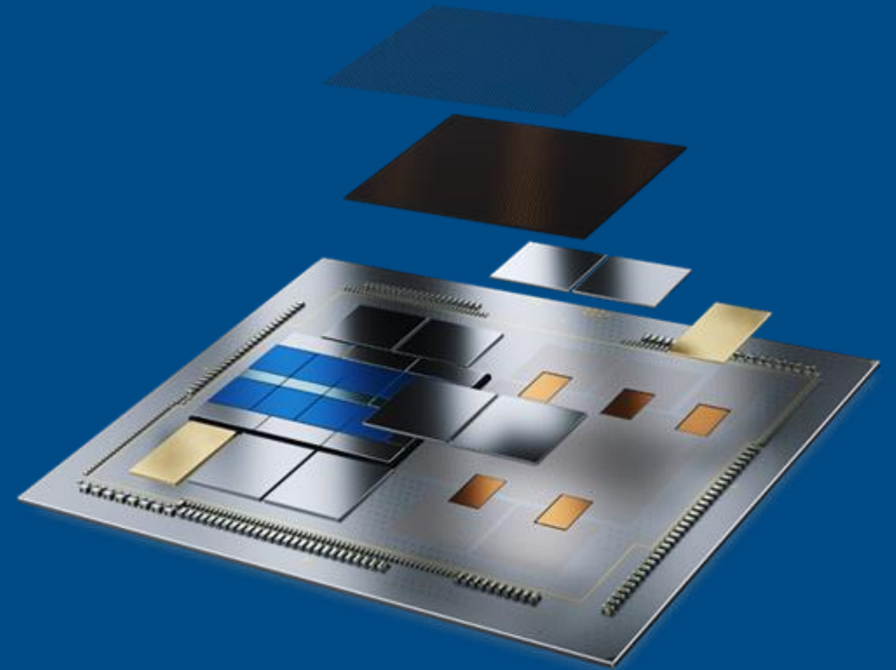
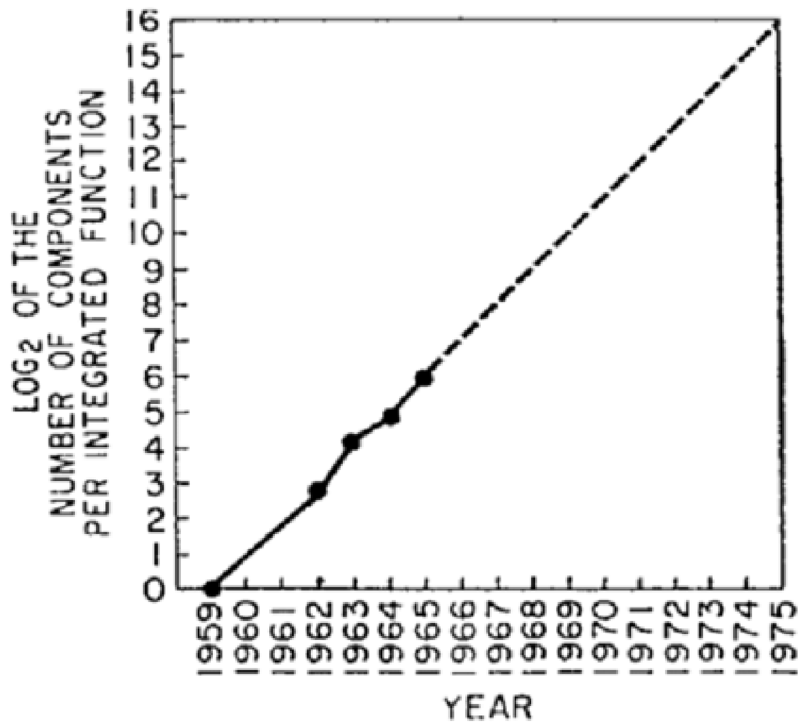


# Agenda

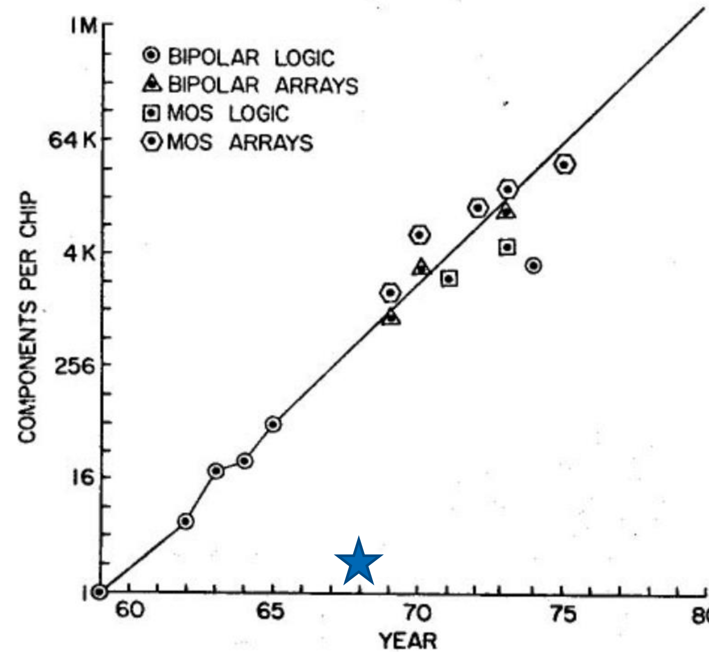
- Moore's Law
- Energy Efficiency Scaling and Looming Energy Crisis
- New Compute Trajectories
- Advanced Packaging
- Summary

# Moore's Law – History

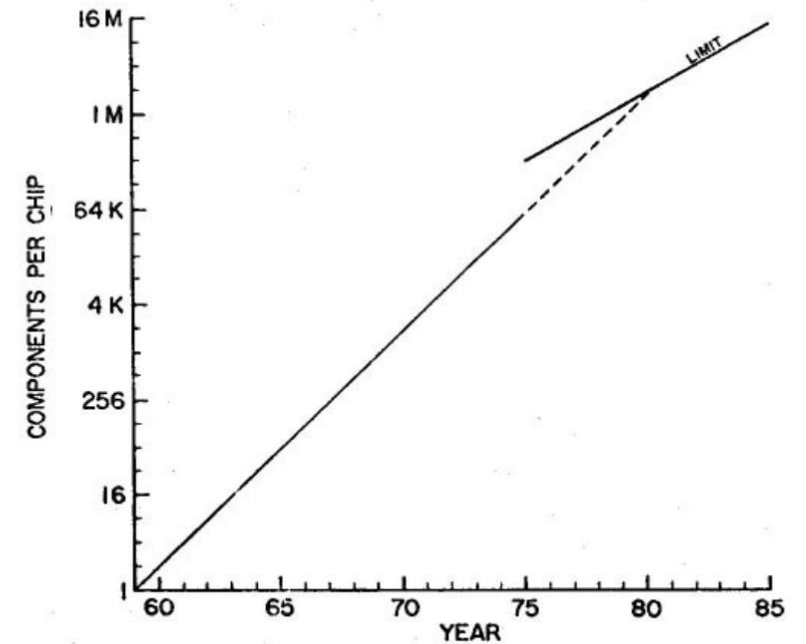
1965 Data and Prediction




1975 Data



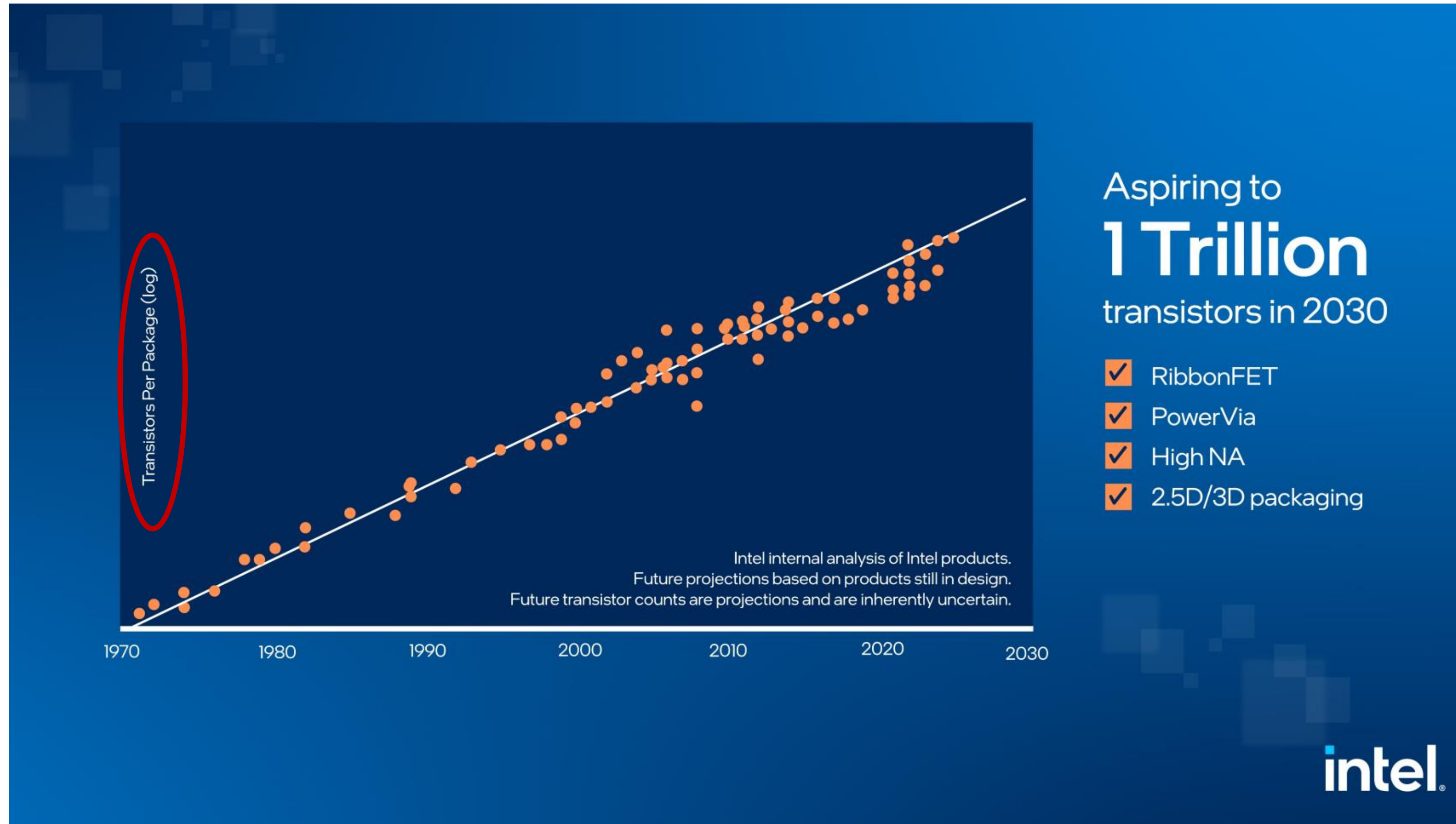

1975 Revised Prediction




- 1965: Number of components (transistors) per chip will double every year
- 1975 revision: Number will double every **two** years

**Sources:**
Gordon Moore, "Cramming more components onto integrated circuits," *Electronics*, 1965; and "Progress in digital integrated electronics," *Digest IEDM*, 1975

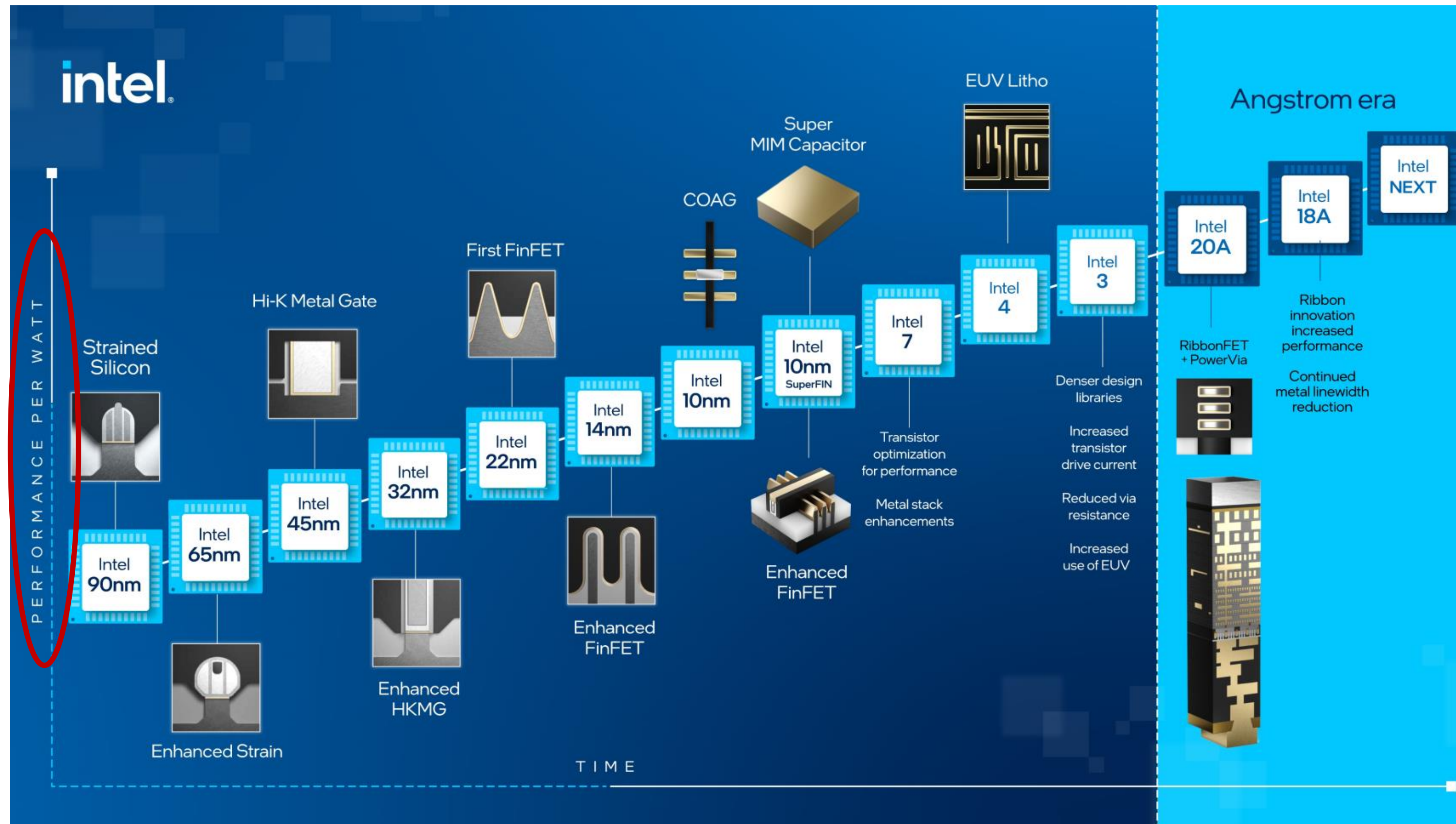
# Moore's Law – Today




**Source:** Ann Kelleher, "Moore's Law – now and in the future," *Intel Newsroom,* 2022

- Moore's Law enabled unprecedented functionality scaling – but what about power?

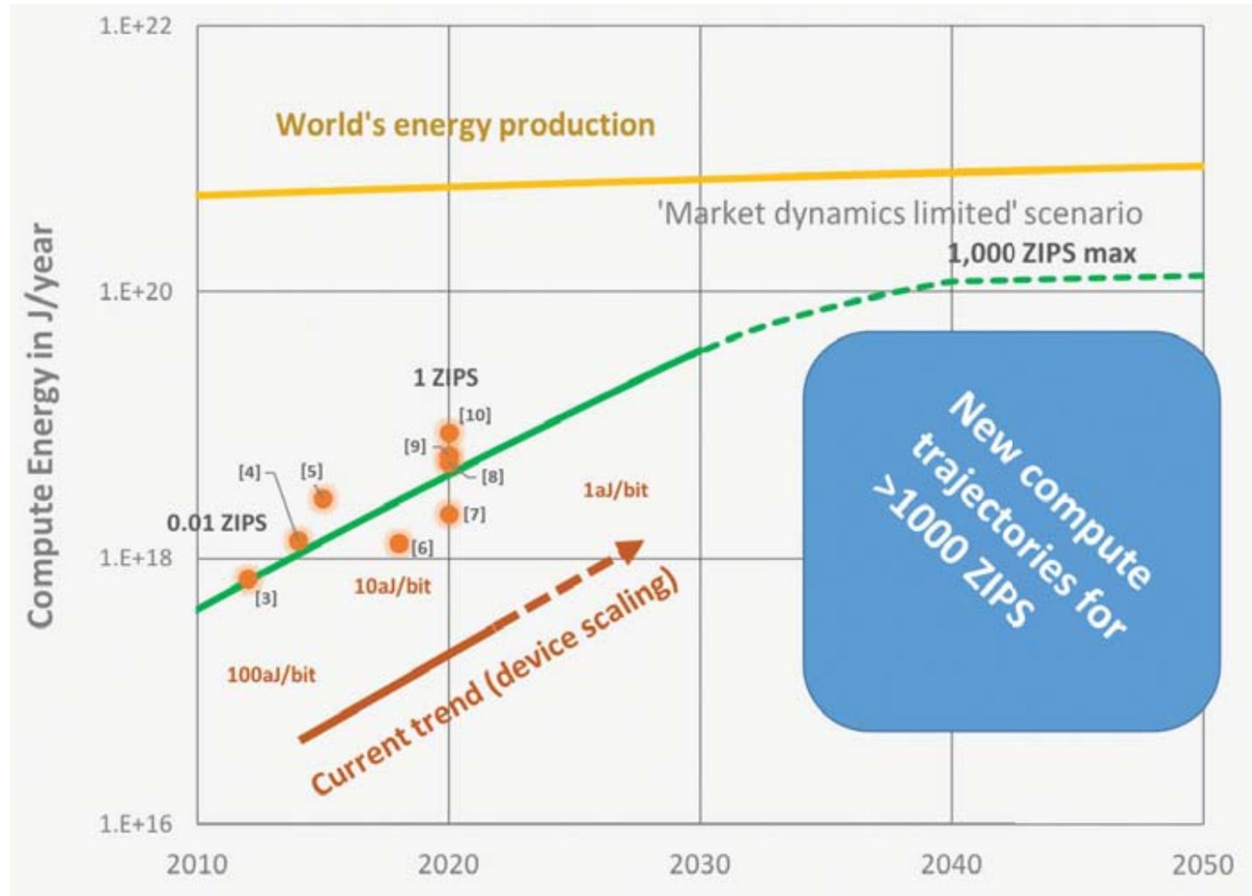
# Energy Effciency Scaling Enabled by Moore’s Law




**Source:** *Ibid.*

- Shrinking transistor devices along with new materials & geometries also enabled exponential growth of performance per watt of power

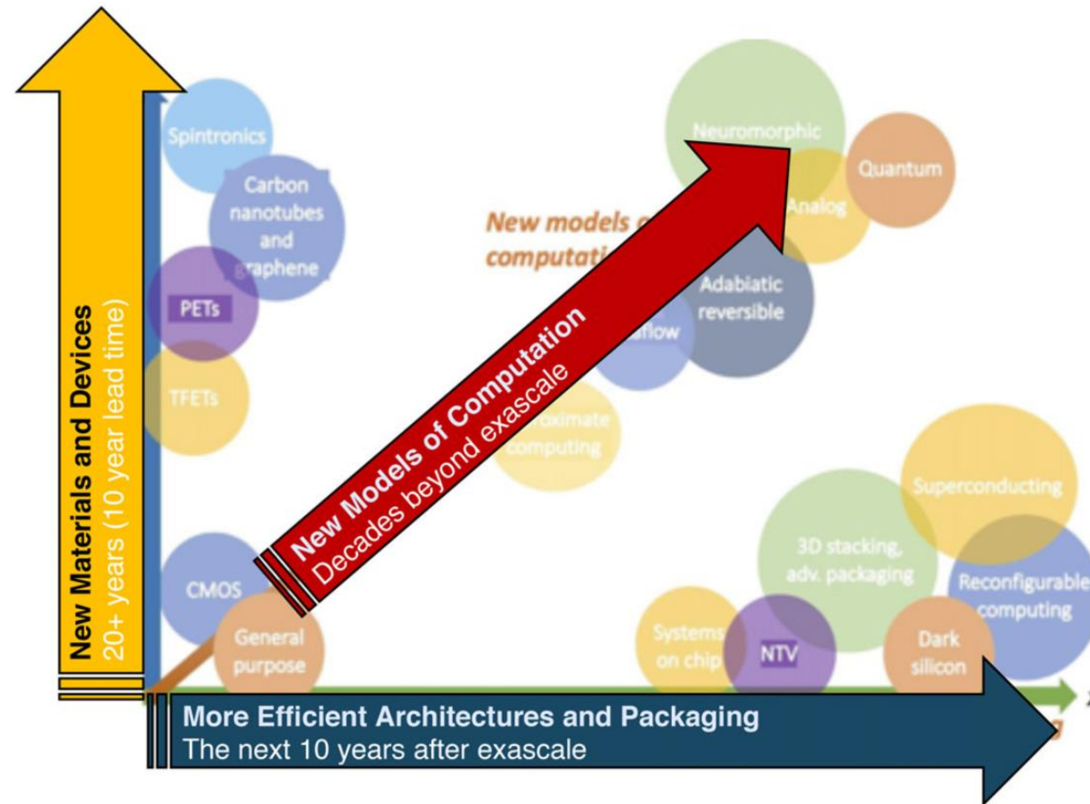
# Current Computing Growth Trend Not Sustainable




**Source:** Semiconductor Research Corporation (SRC), *Decadal Plan for Semiconductors*, 2021

- The demand for computation growth may be outpacing the progress realized by Moore's Law

# New Compute Trajectories




**Source:** John Shalf, “The future of computing beyond Moore’s Law,” *Philosophical Trans.*, 2020

- While research for beyond-CMOS computing is going on to enable new trajectories, advanced packaging steps into the limelight as a key vector for continued advancements

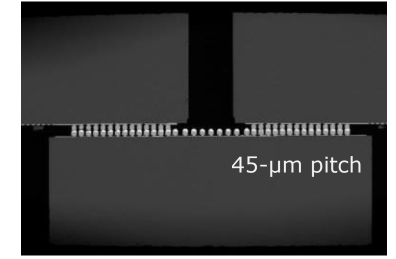
# Microelectronic Packaging

**Source:**
*Ibid.* (Kelleher, 2022)

- Packaging has key electrical, thermal, and mechanical functions to enable Moore's Law scaling

# What Is "Advanced" Packaging?

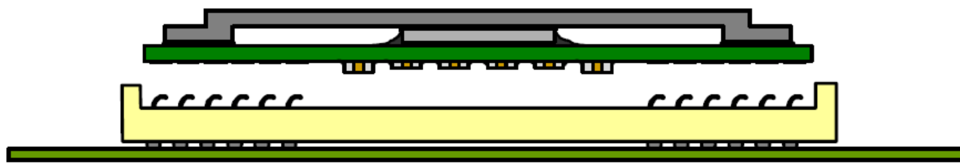
Early Silicon Bridge Prototype




## Conventional Packaging:

- Single or few dies on single package substrate

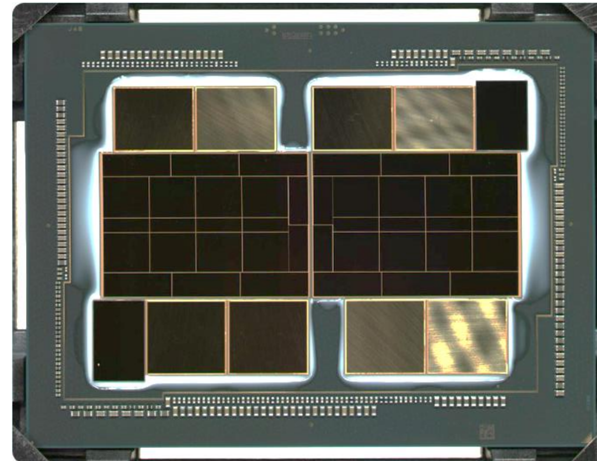
Land Grid Array (LGA) Package and Socket



Microprocessor LGA Package

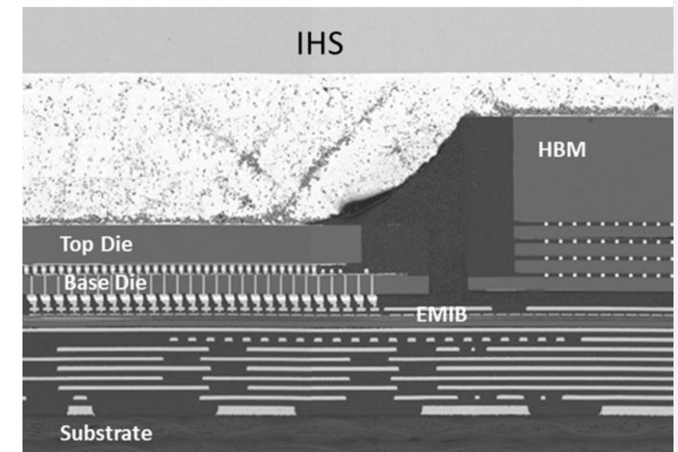
## Advanced Packaging:

- Many dies with 3D stacking at possibly multiple levels



Ponte Vecchio for High-Performance Computing (HPC) and Artificial Intelligence (AI)

Deep Heterogeneous Integration




**Sources:** Henning Braunisch, "High-bandwidth microprocessor packaging," *UWEE Research Colloquium Series,* 2014; Babak Sabi, "Advanced packaging architectures: Opportunities and challenges," *Electronics Packaging Symp.,* 2021; Henning Braunisch *et al.*, "High-speed performance of Silicon Bridge die-to-die interconnects," *Proc. EPEPS*, 2011

# Summary

- Moore's Law scaling has enabled decades of exponential advancements in microelectronic functionality & performance
- Microelectronic packaging is a key vector for enabling further scaling
- Advanced packaging combines many dies with 3D stacking at possibly multiple levels
- This enables heterogeneous integration for more efficient power delivery & thermal management and more efficient data movement
  - Orders of magnitude improvement in terms of energy efficiency may be possible
  - Much work remains to be done. Interdisciplinary and industry-wide collaboration are needed.

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